TPS23861 IEEE 802.3at Quad Port Power-over-Ethernet PSE Controller

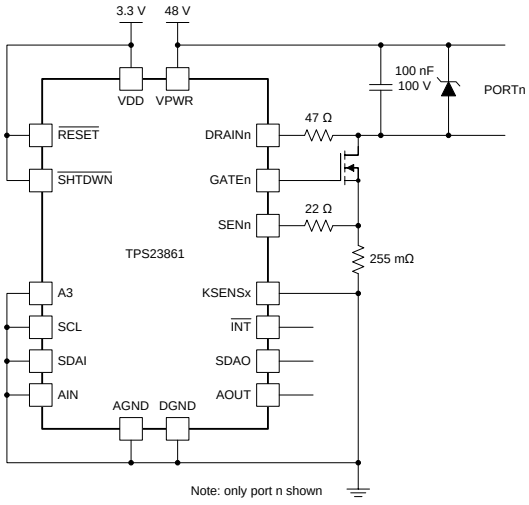
1 Features

- IEEE 802.3at Quad Port PSE Controller
  - Auto Detect, Classification
  - Auto Turn-On and Disconnect
  - Efficient 255-mΩ Sense Resistor
- Pin-Out Enables Two-Layer PCB
- Kelvin Current Sensing
- 4-Point Detection
- Automatic Mode – As Shipped
  - No External Terminal Setting Required
  - No Initial I^2C Communication Required
- Semi-Automatic Mode – Set by I^2C Command
  - Continuous Identification and Classification
  - Meets IEEE 400-ms T_{PON} Specification
  - Fast-Port Shutdown Input
  - Operates best when used in conjunction with system reference code http://www.ti.com/product/TPS23861/toolssoftware
- Optional I^2C Control and Monitoring
- –40°C to 125°C Temperature Range
- TSSOP28 Package 9.8 mm x 6.6 mm

2 Applications

- Ethernet Switches and Routers
- Surveillance NVR and DVRs
- Residential Gateways
- PoE Pass-Through Systems
- Wireless Backhaul

Simplified Schematic



3 Description

The TPS23861 is an easy-to-use, flexible, IEEE802.3at PSE solution. As shipped, it automatically manages four 802.3at ports without the need for any external control.

The TPS23861 automatically detects Powered Devices (PDs) that have a valid signature, determines power requirements according to classification and applies power. Two-event classification is supported for type-2 PDs. The TPS23861 supports DC disconnection and the external FET architecture allows designers to balance size, efficiency and solution cost requirements.

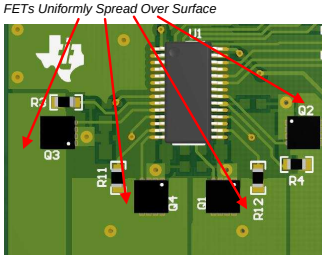
The unique pin-out enables 2-layer PCB designs via logical grouping and clear upper and lower differentiation of I^2C and power pins. This delivers best-in-class thermal performance, Kelvin accuracy and low-build cost.

In addition to automatic operation, the TPS23861 supports Semi-Auto Mode via I^2C control for precision monitoring and intelligent power management. Compliance with the 400-ms T_{PON} specification is ensured whether in semi-automatic or automatic mode.

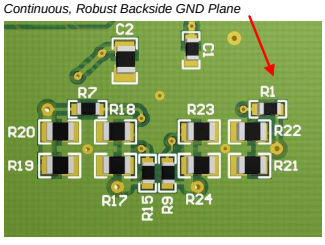
Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
TPS23861PW	TSSOP (28)	9.80 mm x 6.60 mm

TOP CONDUCTORS
FETs Uniformly Spread Over Surface



BOTTOM GND PLANE
Continuous, Robust Backside GND Plane



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4 Revision History

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Changes from Revision D (September 2015) to Revision E — **Page**

- Added note in Features, "Semi-Automatic Mode " ... 1
- Aligned format ... 1
- Updated *Pin Functions* table ... 4
- Added new Figure 37 ... 21
- Added new Functional Block Diagram ... 24
- Changed note in A/D Converter and I²C Interface ... 33
- Changed the Note in I²C Slave Address and AUTO Bit Programming ... 36
- Added note to I²C Slave Address and AUTO Bit Programming ... 36
- Changed I²C slave address register note. ... 36
- Added new Figure 43 ... 40
- Added a note to Manual about type 2 power 2 event classification. ... 41
- Added content to Semi-Auto ... 42
- Added "PoEPn" column to Bits Description ... 72
- Added a note to PoE Plus Register ... 79

Changes from Revision C (June 2015) to Revision D — **Page**

- Added reference note to Figure 5 ... 14
- Added reference note to Figure 6 ... 14
- Changed $\overline{\text{RESET}}$ note to add addition reference link. ... 22
- Added SDAO pin note. ... 23
- Changed I²C Slave Address and AUTO Bit Programming note. ... 36
- Added Figure 42, I²C/SMBus Interface Slave Address Programming Protocol. ... 39

- Added note 3 to Table 10 47
- Changed Connections on Unused Ports section..... 88
- Added reference link to the VPWR-RESET Sequencing note. 99

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- Added Figure 6 14
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- Changed maximum VDD supply current from 10 mA to 6 mA in first paragraph and changed wording in second paragraph of VDD..... 99
- Added VPWR-RESET Sequencing 99

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- Changed VDD current consumption from 10 mA (MAX) to 6.0 mA (MAX)..... 6
- Deleted Processor watchdog trip delay specification..... 10
- Added When using the I^2C interface note. 33
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- Changed FULL SCALE VALUE from 146.2°C to 150°C (typical). 73
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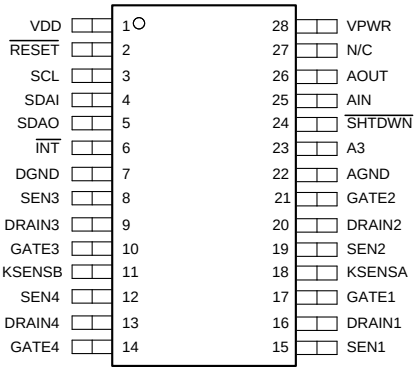
- Added Temperature sensor performance note..... 73

Changes from Original (March 2014) to Revision A **Page**

- Added full TPS23861 IEEE 802.3at Quad Port Power-over-Ethernet PSE Controller datasheet. 1

5 Pin Configuration and Functions

PW Package
28-Pin TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A3	23	I	I^2C A3 address line. Internally pulled up to VDD.
AGND	22	P	Analog ground.
AIN	25	I	I^2C address programming input line; this pin is internally pulled up to VDD.
AOUT	26	O	I^2C address programming line; this output is open drain.
DGND	7	P	Digital ground.
DRAIN3	9	I	Port 1-4 output voltage monitor; connect to output port through a 47-Ω resistor.
DRAIN4	13	I	
DRAIN1	16	I	
DRAIN2	20	I	
GATE3	10	O	Port 1-4 gate-drive output.
GATE4	14	O	
GATE1	17	O	
GATE2	21	O	
$\overline{INT}$	6	O	Interrupt; this pin asserts low when a bit in the interrupt register is asserted. This pin is updated between I^2C transactions. This output is open drain.
KSENSA	18	I	Kelvin point connection for SEN1 and SEN2.
KSENSB	11	I	Kelvin point connection for SEN3 and SEN4.
N/C	27	x	Used to effect regulatory voltage-spacing compliance. Leave this pin open.
$\overline{RESET}$	2	I	Reset; when asserted low, the device resets. This pin is internally pulled up to VDD.
SCL	3	I	Serial clock input for I^2C bus.
SDAI	4	I	Serial data input for I^2C bus; this pin can be connected to SDAO for non-isolated systems.
SDAO	5	O	Serial data output for I^2C bus; this pin can be connected to SDAI for non-isolated systems. This output is open drain.
SEN3	8	I	Port 1-4 current-sense input; connect to current-sense resistor through a 22-Ω resistor.
SEN4	12	I	
SEN1	15	I	
SEN2	19	I	
$\overline{SHTDWN}$	24	I	Low-priority ports shutdown.
VDD	1	P	Digital 3.3-V supply. Bypass VDD to DGND using a 0.1-µF capacitor.
VPWR	28	P	Analog 48-V supply. Bypass VPWR to AGND using a 0.1-µF capacitor.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature, voltages are referenced to DGND and AGND tied together (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	VPWR	–0.3	70	V
Input voltage	VDD	–0.3	4	V
Voltage	AGND	–0.3	0.3	V
Voltage	SDAI, SDAO(2), SCL, AIN, AOUT, $\overline{\text{SHTDWN}}$, $\overline{\text{RESET}}$, $\overline{\text{INT}}$, A3(2)	–0.3	4	V
Output voltage	GATE1-4 (3)(4)	–0.3	13	V
Input voltage	SEN1-4(5), KSENSA, KSENSB	–0.3	3	V
Voltage	DRAIN1-4(2)(6)	–0.3	70	V
Voltage	N/C pin	0	70	V
Sinking current	$\overline{\text{INT}}$, SDAO		20	mA
Lead temperature 1.6 mm (1/16-inch) from case for 10 seconds			260	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Do not apply external voltage sources directly.
(3) Application of voltage is not implied – these are internally driven pins.
(4) If there is a short between drain and gate, the GATE pin may internally permanently disconnect to prevent cascade damage. The three other ports will continue to operate.
(5) SEN1-4 will be tolerant to 15-V transients to avoid fault propagation when a MOSFET fails in short-circuit.
(6) Short transients (µs range) up to 80 V are allowed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature, voltages are referenced to DGND (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VDD}		3.0	3.3	3.6	V
V_{VPWR}		44	48	57	V
	Voltage slew rate on DRAIN1-4			1	V/µs
T_J	Operating junction temperature	-40		125	°C
T_A	Operating free-air temperature	-40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS23861 PW (TSSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	70.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	27.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

–40 ≤ T_J ≤ +125°C, V_{VDD} = 3.3 V, V_{VPWR} = 48 V, V_{DGND} = V_{AGND}, DGND, KSENSA and KSENSB connected to AGND, and all outputs are unloaded, PoEPn = 0, Positive currents are into pins, R_S = 0.255 Ω, to KSENSA (SEN1 or SEN2) or to KSENSB (SEN3 or SEN4), R_{SENS} = 22 Ω, R_{DRAIN} = 47 Ω, typical values are at 25°C. All voltages are with respect to AGND, operating registers loaded with default values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY VPWR						
I_{VPWR}	VPWR current consumption	V_{VPWR} = 57 V		3.5	7	mA
V_{UVLOPW_F}	VPWR UVLO falling threshold	Internal oscillator stops operating	14.5		17.5	V
V_{PUV_F}	VPWR Undervoltage falling threshold	V_{PUV} for port de-assertion	25	26.5	28	V
V_{UVLOPW_R}	VPWR UVLO rising threshold		15.5		18.5	V
INPUT SUPPLY VDD						
I_{VDD}	VDD current consumption			5	6	mA
V_{UVDD_F}	VDD UVLO falling threshold	For port turn off	2	2.2	2.4	V
V_{UVDD_R}	VDD UVLO rising threshold		2.4	2.6	2.8	V
V_{UVDD_HYS}	Hysteresis VDD UVLO(1)			0.4		V
DETECTION						
I_{DET}	Detection current	First detection point, $V_{VPWR} - V_{DRAINn}$ = 0 V	145	160	190	µA
		2nd detection point, $V_{VPWR} - V_{DRAINn}$ = 0 V	235	270	300	µA
		High Current detection point, $V_{VPWR} - V_{DRAINn}$ = 0 V	490	540	585	µA
ΔI_{DET}	2nd – 1st detection currents	At $V_{VPWR} - V_{DRAINn}$ = 0 V	98	110	118	µA
V_{detect}	Open circuit detection voltage	$V_{VPWR} - V_{DRAINn}$	17.5	19	22	V
R_{REJ_LOW}	Rejected resistance low range		0.85		15	kΩ
R_{REJ_HI}	Rejected resistance high range		33		50	kΩ
R_{ACCEPT}	Accepted resistance range		19	25	26.5	kΩ
R_{SHORT}	Shorted port threshold				350	Ω
R_{OPEN}	Open port threshold		55			kΩ
CLASSIFICATION						
V_{CLASS}	Classification voltage	$V_{VPWR} - V_{DRAINn}$, V_{SENn} ≥ 0 mV , I_{port} ≥ 180 µA,	15.5	18.5	20.5	V
I_{CLASS_Lim}	Classification current limit	$V_{VPWR} - V_{DRAINn}$ = 0 V		70	90	mA
I_{CLASS_TH}	Classification threshold current	Class 0-1	5		8	mA
		Class 1-2	13		16	mA
		Class 2-3	21		25	mA
		Class 3-4	31		35	mA
		Class 4- overcurrent	45		51	mA
V_{MARK}	Mark voltage	4 mA ≥ I_{port} ≥ 180 µA, $V_{VPWR} - V_{DRAINn}$	7		10	V
I_{MARK_Lim}	Mark sinking current Limit	$V_{VPWR} - V_{DRAINn}$ = 0 V	10	70	90	mA

(1) These parameters are provided for reference only, and do not constitute part of TI's published specifications for purposes of TI's product warranty.

Electrical Characteristics (continued)

–40 ≤ T_J ≤ +125°C, V_{VDD} = 3.3 V, V_{VPWR} = 48 V, V_{DGND} = V_{AGND}, DGND, KSENSA and KSENSB connected to AGND, and all outputs are unloaded, PoEPn = 0, Positive currents are into pins, R_S = 0.255 Ω, to KSENSA (SEN1 or SEN2) or to KSENSB (SEN3 or SEN4), R_{SENS} = 22 Ω, R_{DRAIN} = 47 Ω, typical values are at 25°C. All voltages are with respect to AGND, operating registers loaded with default values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GATE						
V_{GOH}	Gate drive voltage	V_{GATEn} , I_{GATE} = –1 µA	10		12.5	V
I_{GO-}	Gate sinking current with power-on reset, shutdown detected or port turn off command	V_{GATEn} = 5 V	80	100	150	mA
$I_{GO\ short-}$	Gate sinking current with port short-circuit	V_{GATEn} = 5 V, V_{SENn} ≥ V_{SHORT} (or $V_{SHORT2X}$ if 2x mode)	80	100	150	mA
I_{GO+}	Gate sourcing current	V_{GATEn} = 0 V, IGATE = 0	39	50	63	µA
		IGATE = 1	18	25	34	µA
DRAIN INPUT						
V_{PGT}	Power good threshold	Measured at V_{DRAINn}	1.0	2.13	3	V
V_{SHT}	Shorted FET threshold	Measured at V_{DRAINn}	4	6	8	V
R_{DRAIN}	Resistance from DRAINn to VPWR	Any operating mode except during detection or while the port is ON, including in device reset state	80	100	190	kΩ
I_{DRAIN}	DRAINn pin bias current	V_{DRAINn} = 48 V, port OFF (not in detection)			1	µA
		V_{VPWR} - V_{DRAINn} = 30 V, port ON		75	100	µA
A/D CONVERTER						
T_{CONV}	Conversion time , A/D #1 to 4	All ranges, each port current	0.65	0.8	1	ms
A_{DCBW} (1)	ADC integration bandwidth (–3 dB) (1)			320		Hz
T_{INT_CUR}	Integration (averaging) time, current	Each port, port ON current	80	100	125	ms
T_{INT_DET}	Integration (averaging) time, detection (1)	MAINS bit = 0			20	ms
	Powered port voltage conversion scale factor and accuracy	At V_{VPWR} – V_{DRAINn} = 57 V, 0°C to 125°C	15175	15565	15955	Counts
		At V_{VPWR} – V_{DRAINn} = 44 V, 0°C to 125°C	11713	12015	12316	Counts
		At V_{VPWR} – V_{DRAINn} = 57 V, –40°C to 125°C	15020	15565	16110	Counts
		At V_{VPWR} – V_{DRAINn} = 44 V, –40°C to 125°C	11594	12015	12436	Counts
	Powered port current conversion scale factor and accuracy	At port current = 770 mA	12300	12616	12932	Counts
		At port current = 7.5 mA	90	123	156	Counts
	Input voltage conversion scale factor and accuracy	At V_{VPWR} = 57 V	15175	15565	15955	Counts
		At V_{VPWR} = 44 V	11713	12015	12316	Counts
V_{OS}	Powered port voltage conversion offset	At V_{VPWR} – V_{DRAINn} = 0.3 V	0		600	mV
δ_V/V_{PORT}	Voltage reading accuracy	At 44 V to 57 V –40°C to 125°C	–3.5%		3.5%	
		At 44 V to 57 V 0°C to 125°C	–2.5%		2.5%	
δ_I/I_{port}	Current reading accuracy	At 50 mA to 770 mA	–2.5%		2.5%	

Electrical Characteristics (continued)

–40 ≤ T_J ≤ +125°C, V_{VDD} = 3.3 V, V_{VPWR} = 48 V, V_{DGND} = V_{AGND}, DGND, KSENSA and KSENSB connected to AGND, and all outputs are unloaded, PoEPn = 0, Positive currents are into pins, R_S = 0.255 Ω, to KSENSA (SEN1 or SEN2) or to KSENSB (SEN3 or SEN4), R_{SENS} = 22 Ω, R_{DRAIN} = 47 Ω, typical values are at 25°C. All voltages are with respect to AGND, operating registers loaded with default values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PORT CURRENT SENSE						
V_{CUT}	I_{CUT} limit	V_{DRAINn} = 0 V, I_{CUT} port n[2:0] = 000, default	90.60	95.37	100.14	mV
		V_{DRAINn} = 0 V, I_{CUT} port n[2:0] = 001	26.65	28.05	29.45	mV
		V_{DRAINn} = 0 V, I_{CUT} port n[2:0] = 010	49.42	52.02	54.62	mV
		V_{DRAINn} = 0 V, I_{CUT} port n[2:0] = 110	156.27	164.5	172.72	mV
		V_{DRAINn} = 0 V, I_{CUT} port n[2:0] = 111	222.87	234.6	246.33	mV
δ_{ICUT}/I_{CUT}	I_{CUT} tolerance		–5%		5%	
V_{INRUSH}	I_{Inrush} limit	At port turn on, $V_{VPWR} – V_{DRAINn}$ = 1 V	10	23	31	mV
		V_{VPWR} - V_{DRAINn} = 10 V	20	33	46	mV
		V_{VPWR} - V_{DRAINn} = 30 V	102		114.7	mV
		$V_{VPWR} – V_{DRAINn}$ = 55 V	102		114.7	mV
V_{LIM}	ILIM limit with PoEPn = 0	V_{DRAINn} = 1 V	102		114.7	mV
		V_{DRAINn} = 13 V	102		114.7	mV
		V_{DRAINn} = 30 V	15	23	31	mV
		V_{DRAINn} = 48 V	15	23	31	mV
V_{LIM2X}	ILIM limit with PoEPn = 1	V_{DRAINn} = 1 V	260	270.3	285	mV
		V_{DRAINn} = 10 V	127	140	153	mV
		V_{DRAINn} = 30 V	15	23	31	mV
		V_{DRAINn} = 48 V	15	23	31	mV
V_{SHORT}	I_{SHORT} threshold with PoEPn = 0	Threshold for GATE to be less than 1 V, 2 µs after application of pulse	140		183	mV
$V_{SHORT2X}$	I_{SHORT} threshold with PoEPn = 1		357		408	mV
I_{BIAS}	Sense pin bias current	Port ON or during class	-2.25		0	µA
$V_{I(min)}$	Disconnect threshold	DCTHn = 00, default	1.275		2.55	mV
		DCTHn = 01	2.55		5.1	mV
		DCTHn = 10	5.1		10.2	mV
		DCTHn = 11	8.5		17	mV

Electrical Characteristics (continued)

–40 ≤ T_J ≤ +125°C, V_{VDD} = 3.3 V, V_{VPWR} = 48 V, V_{DGND} = V_{AGND}, DGND, KSENSA and KSENSB connected to AGND, and all outputs are unloaded, PoEPn = 0, Positive currents are into pins, R_S = 0.255 Ω, to KSENSA (SEN1 or SEN2) or to KSENSB (SEN3 or SEN4), R_{SENS} = 22 Ω, R_{DRAIN} = 47 Ω, typical values are at 25°C. All voltages are with respect to AGND, operating registers loaded with default values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INTERFACE AT V_{VDD} = 3.3 V						
V_{IH}	Digital input high		2.1			V
V_{IL}	Digital input low				0.9	V
V_{IT_HYS}	Input voltage hysteresis (SCL, SDAI, AIN, A3, $\overline{\text{RESET}}$, $\overline{\text{SHTDWN}}$)		0.17			V
V_{OL}	Digital output Low, SDAO	I_{OL} = 9 mA			0.4	V
	Digital output Low, $\overline{\text{INT}}$	I_{OL} = 3 mA			0.4	V
R_{pullup}	Pullup resistor to VDD	$\overline{\text{RESET}}$, AIN, A3, $\overline{\text{SHTDWN}}$	30	50	80	kΩ
AOUT OUTPUT						
V_{OL_AOUT}	AOUT output low voltage	During slave address programming, I_{AOUT} = 1 mA			0.7	V
EEPROM (I^2C Slave Address)						
n_{EE_cyc}	EEPROM endurance	40 V < V_{VPWR} < 57 V	25			cycles
t_{WC}	Write cycle time (byte or page)	40 V < V_{VPWR} < 57 V		10	100	ms
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature	Temperature rising	143	154	161	°C
	Hysteresis(1)			8		°C

6.6 Timing Requirements

–40 ≤ T_J ≤ +125°C, V_{VDD} = 3.3 V, V_{VPWR} = 48 V, V_{DGND} = V_{AGND}, DGND, KSENSA and KSENSB connected to AGND, and all outputs are unloaded, PoEPn = 0, Positive currents are into pins, R_S = 0.255 Ω, to KSENSA (SEN1 or SEN2) or to KSENSB (SEN3 or SEN4), R_{SENS} = 22 Ω, R_{DRAIN} = 47 Ω, typical values are at 25°C. All voltages are with respect to AGND, operating registers loaded with default values (unless otherwise noted)

		MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency	10		400	kHz
t_{LOW}	LOW period of SCL clock	1.3			µs
t_{HIGH}	HIGH period of SCL clock	0.6			µs
t_{fo}	SDAO output fall time, SDAO, 2.3 → 0.8 V, C_b = 10 pF, 10-kΩ pullup to 3.3 V	21		250	ns
	SDAO output fall time, SDAO, 2.3 → 0.8 V, C_b = 400 pF, 1.3-kΩ pullup to 3.3 V	60		250	ns
C_{I2C}	SCL capacitance			10	pF
C_{I2C_SDA}	SDAI, SDAO capacitance			6	pF
$t_{SU,DATW}$	Data set-up time (write operation)	100			ns
$t_{SU,DATR}$	Data set-up time (read operation), SDAO, 2.3 ↔ 0.8 V, C_b = 400 pF, 1.3-kΩ pull up to 3.3 V	600			ns
$t_{HD,DATW}$	Data hold time (write operation)	0			ns
$t_{HD,DATR}$	Data hold time (read operation)	150		600	ns
t_{fSDA}	Input fall times of SDAI, 2.3 → 0.8 V	20		250	ns
t_{rSDA}	Input rise times of SDAI, 0.8 → 2.3 V	20		300	ns
t_r	Input rise time of SCL, 0.8 → 2.3 V	20		300	ns
t_f	Input fall time of SCL, 2.3 → 0.8 V	20		200	ns
t_{BUF}	Bus free time between a stop and start condition	1.3			µs
$t_{HD,STA}$	Hold time after (repeated) start condition	0.6			µs
$t_{SU,STA}$	Repeated start condition set-up time	0.6			µs
$t_{SU,STO}$	Stop condition set-up time	0.6			µs
$t_{FLT\_\overline{INT}}$ (1)	Fault to $\overline{INT}$ assertion, Time to internally register an interrupt in response to a fault		150		µs
$t_{ARA\_\overline{INT}}$	ARA to $\overline{INT}$ negation			500	ns
t_{DG}	Suppressed spike pulse width, SDAI and SCL	50			ns
t_{RDG}	$\overline{RESET}$ input minimum pulse width (deglitch time)			5	µs
t_{WDT_I2C}	I^2C Watchdog trip delay	1.1	2.2	3.3	s
t_{STP_AOUT}	Delay STOP bit to A_{OUT} high during I^2C address programming			1.25	µs

(1) These parameters are provided for reference only, and do not constitute part of TI's published specifications for purposes of TI's product warranty.

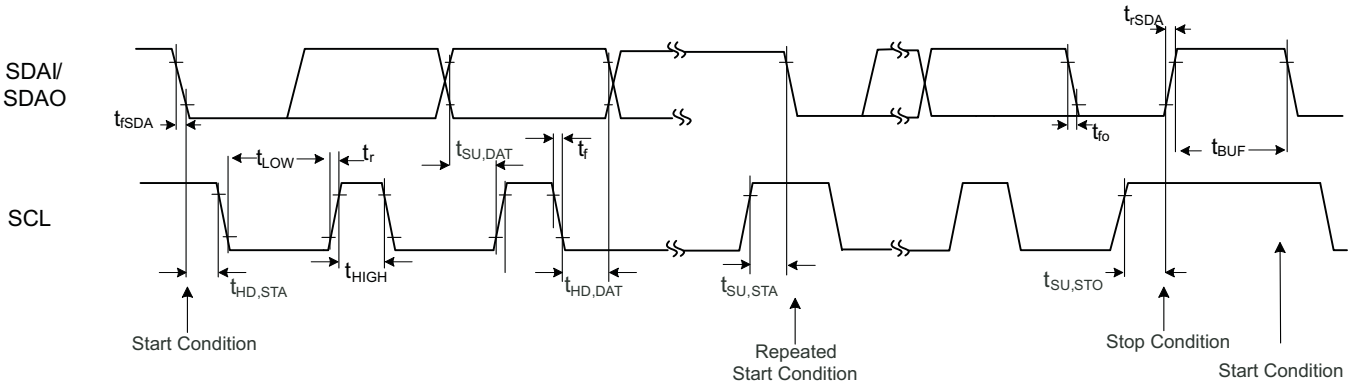


Figure 1. I^2C Timings

6.7 Switching Characteristics

–40 ≤ T_J ≤ +125°C, V_{VDD} = 3.3 V, V_{VPWR} = 48 V, V_{DGND} = V_{AGND}, DGND, KSENSA and KSENSB connected to AGND, and all outputs are unloaded, PoEPn = 0, Positive currents are into pins, R_S = 0.255 Ω, to KSENSA (SEN1 or SEN2) or to KSENSB (SEN3 or SEN4), R_{SENS} = 22 Ω, R_{DRAIN} = 47 Ω, typical values are at 25°C. All voltages are with respect to AGND, operating registers loaded with default values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
δIfault	Duty cycle of I_{PORT} with current fault		5.5%		6.7%	
t_{OVLD}	I_{CUT} time limit	TICUT = 00, default as supplied	50		70	ms
		TICUT = 01	25		35	ms
		TICUT = 10	100		140	ms
		TICUT = 11	200		280	ms
t_{LIM}	ILIM time limit	POEPn = 0, default as supplied	50		70	ms
		POEPn = 1, TLIM = 00	50		70	ms
		POEPn = 1, TLIM = 01	28.4	30	34	ms
		POEPn = 1, TLIM = 10	14.7	15.5	17	ms
		POEPn = 1, TLIM = 11	9.025		11.5	ms
t_{START}	Maximum current limit duration in port start-up	TSTART = 00, default as supplied	50		70	ms
		TSTART = 01	25		35	ms
		TSTART = 10	100		140	ms
t_{DET}	Four-point detection duration	Time to complete a detection	275		500	ms
t_{DET_BOFF}	Pause between detection attempts	V_{VPWR} – V_{DRAINn} > 2.5 V	300	400	500	ms
		V_{VPWR} – V_{DRAINn} < 2.5 V	0		150	ms
t_{CLE}	Classification duration	1st and 2nd class event, Auto Mode, Semi-Auto Mode, from detection complete	6.5		13	ms
t_{pdc}	Classification duration	1-event physical layer class timing, Auto Mode and Semi-Auto Mode, from detection complete	6.5		13	ms
		Manual mode, from beginning of classification	6.5		14	ms
t_{ME}	Mark duration	1st and 2nd mark event, from class 4 complete	6		12	ms
$t_{p(on)}$	Port power-on delay	Manual mode, from port turn-on command to port turn on completed			4	ms

Switching Characteristics (continued)

–40 ≤ T_J ≤ +125°C, V_{VDD} = 3.3 V, V_{VPWR} = 48 V, V_{DGND} = V_{AGND}, DGND, KSENSA and KSENSB connected to AGND, and all outputs are unloaded, PoEPn = 0, Positive currents are into pins, R_S = 0.255 Ω, to KSENSA (SEN1 or SEN2) or to KSENSB (SEN3 or SEN4), R_{SENS} = 22 Ω, R_{DRAIN} = 47 Ω, typical values are at 25°C. All voltages are with respect to AGND, operating registers loaded with default values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ed}	Fault delay timing. Delay before next attempt to power a port following power removal due to fault condition	ICUT , ILIM or start fault, Auto Mode, Semi-Auto Mode, CLDN = 0X, default as supplied	0.8	1	1.2	s
		ICUT , ILIM or start fault, Auto Mode, Semi-Auto Mode, CLDN = 10	1.6	2	2.4	s
		ICUT , ILIM or start fault, Auto Mode, Semi-Auto Mode, CLDN = 11	3.2	4	4.8	s
t_{MPDO}	PD maintain power signature dropout time limit	TDIS = 00, default as supplied	300		400	ms
		TDIS = 01	75		100	ms
		TDIS = 10	150		200	ms
		TDIS = 11	600		800	ms
$t_{D\_off\_\overline{SHDWN}}$	Gate turn-off time from $\overline{SHTDWN}$ input	From $\overline{SHTDWN}$ to V_{GATEn} < 1 V, V_{SENn} = 0 V	1		5	µs
$t_{P\_off\_CMD}$	Gate turn-off time from port off command	From port off command to V_{GATEn} < 1 V, V_{SENn} = 0 V			900	µs
$t_{P\_off\_RST}$	Gate turn-off time with $\overline{RESET}$ pin	From $\overline{RESET}$ low to, V_{GATEn} < 1 V, V_{SENn} = 0 V	1		5	µs
$t_{D\_off\_SEN}$	Gate turn-off time from SENn input	POEPn = 0, V_{DRAINn} = 1 V , from V_{SENn} pulsed to 0.425 V			0.9	µs
		POEPn = 1, V_{DRAINn} = 1 V , from V_{SENn} pulsed to 0.62 V			0.9	µs
t_{POR}	Device power-on-reset delay				23	ms
$t_{\overline{RESET}}$	Reset time duration from $\overline{RESET}$ pin		1		5	µs

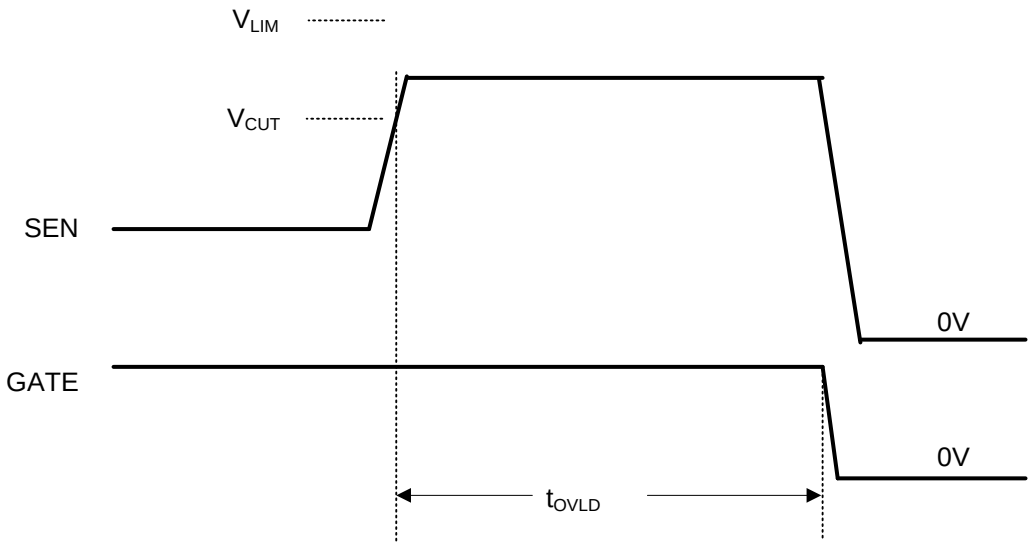


Figure 2. Overcurrent Fault Timing

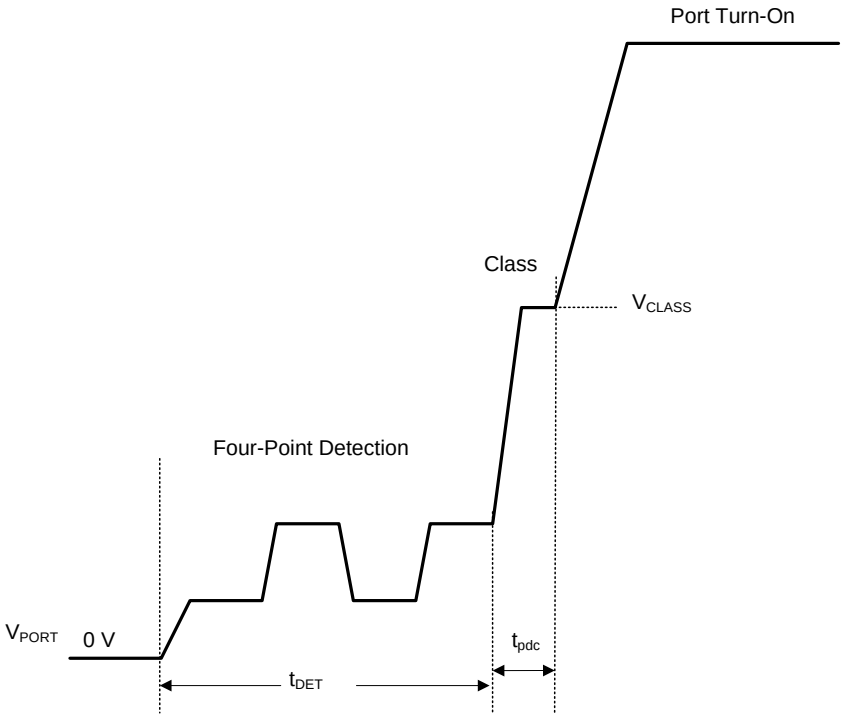


Figure 3. Detection, 1-Event Classification, and Turn On

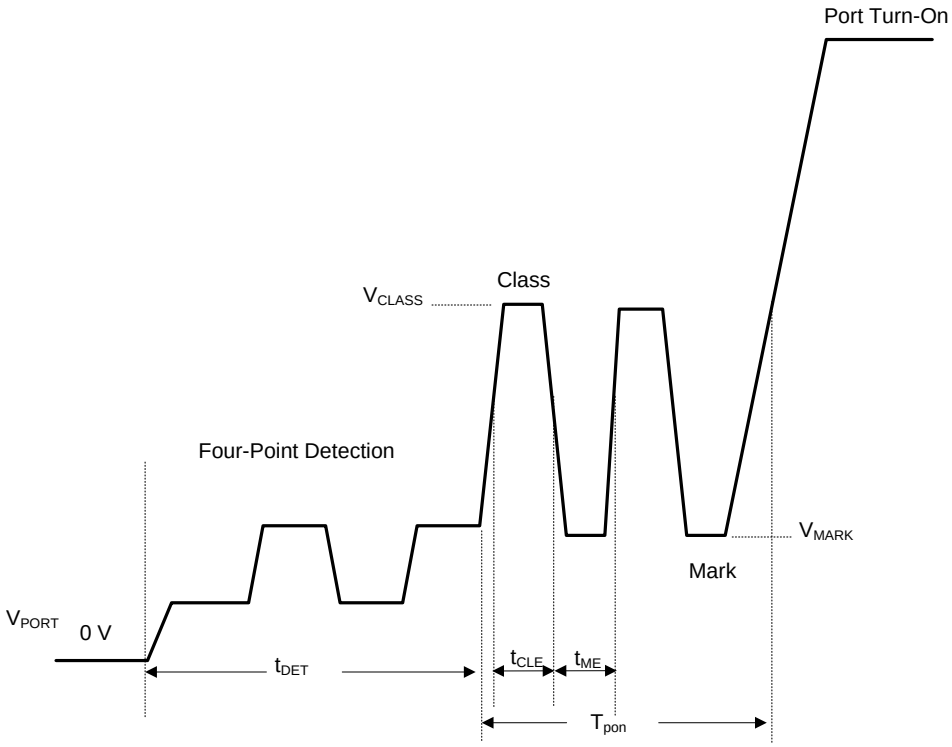


Figure 4. Detection, 2-Event Classification, and Turn On

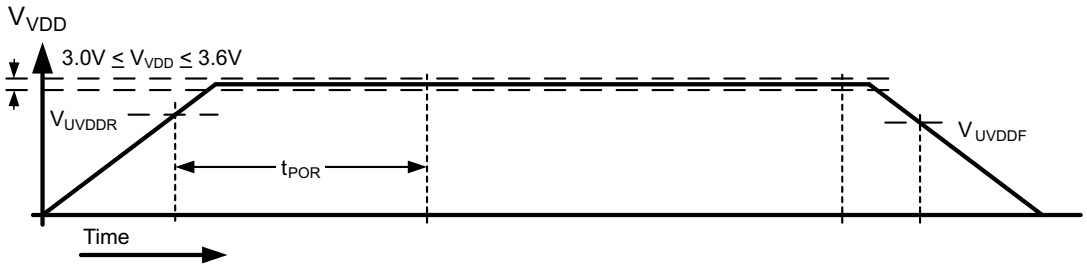


Figure 5. VDD Power-On-Reset
(For more information refer to the application note, TPS23861 Power-On Considerations, SLVA723.)

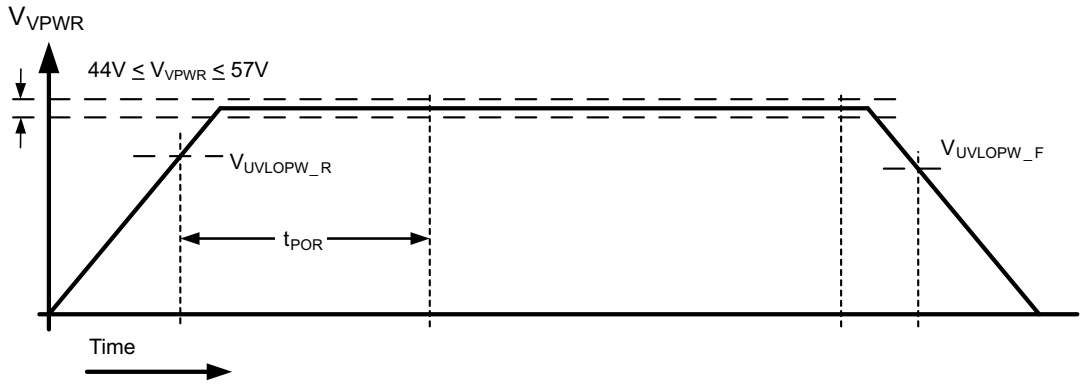


Figure 6. VPWR Power-On-Reset
(For more information refer to the application note, TPS23861 Power-On Considerations, SLVA723.)

6.8 Typical Characteristics

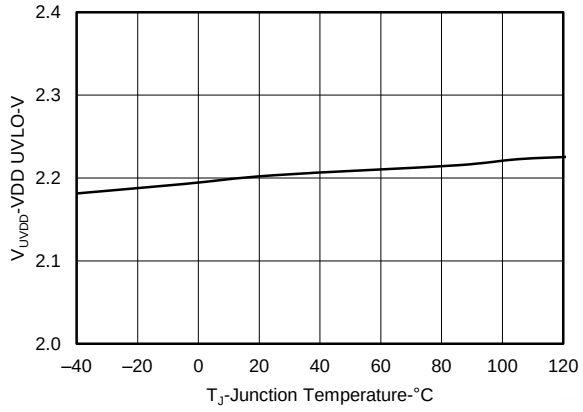


Figure 7. VDD UVLO vs Junction Temperature

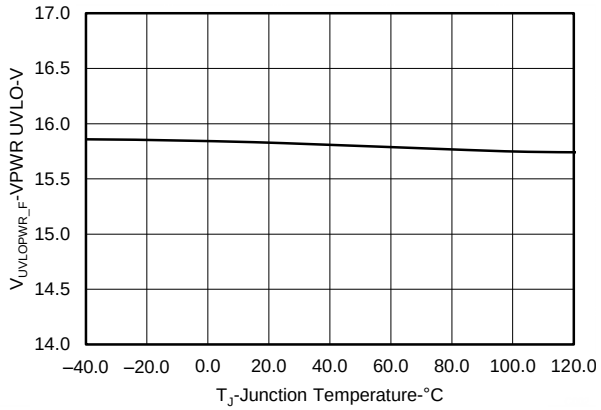


Figure 8. VPWR UVLO vs Junction Temperature

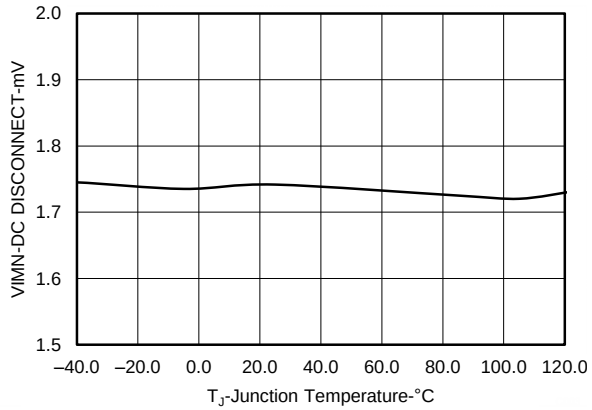


Figure 9. DC Disconnect vs Junction Temperature

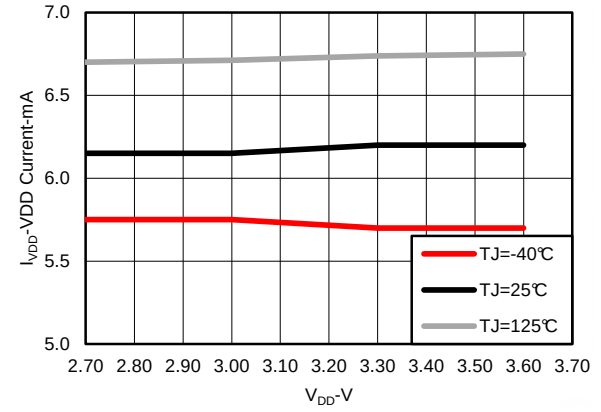


Figure 10. VDD Current vs VDD

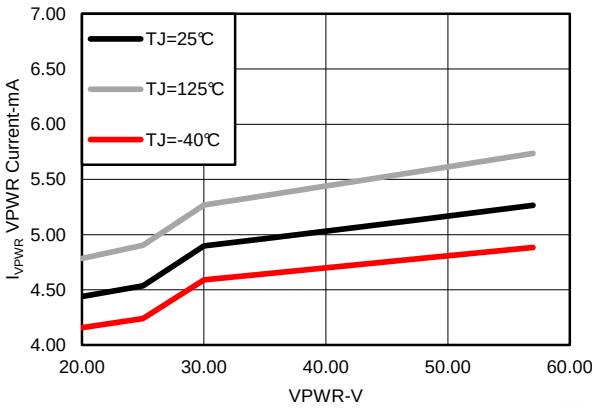


Figure 11. VPWR Current vs VPWR

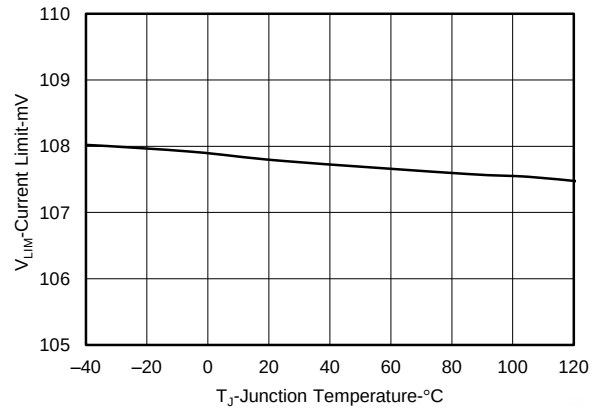


Figure 12. Current Limit (1x threshold) vs Junction Temperature

Typical Characteristics (continued)

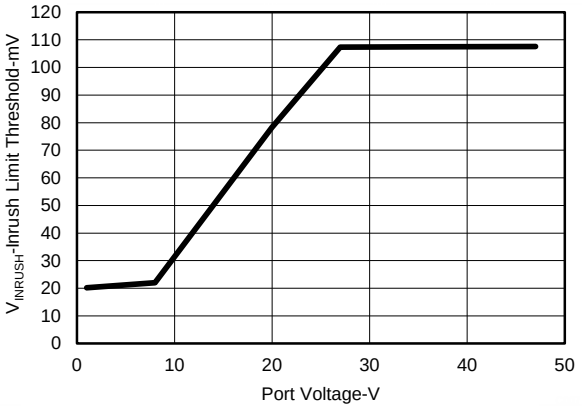


Figure 13. Inrush Current Limit Threshold vs Port Voltage

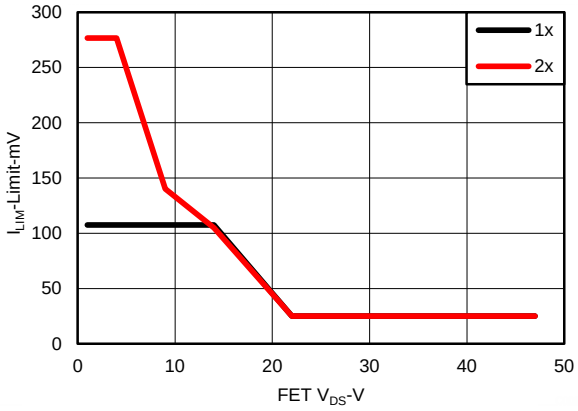


Figure 14. Current Limit Threshold vs FET Voltage

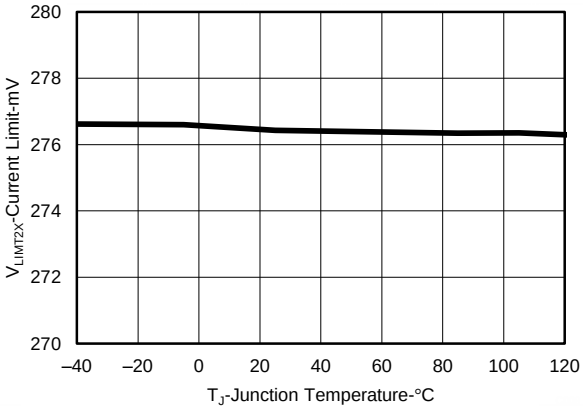


Figure 15. Current Limit (2x threshold) vs Junction Temperature

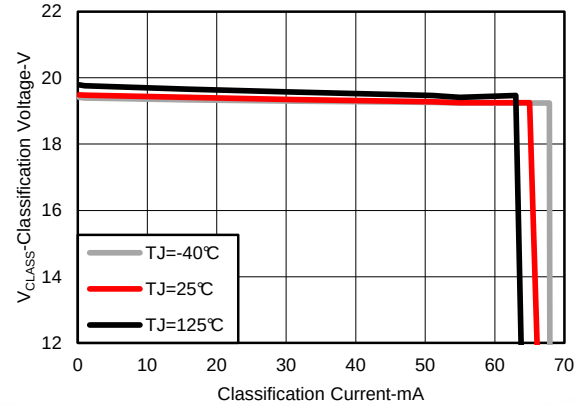


Figure 16. Classification Voltage vs Port Classification Current

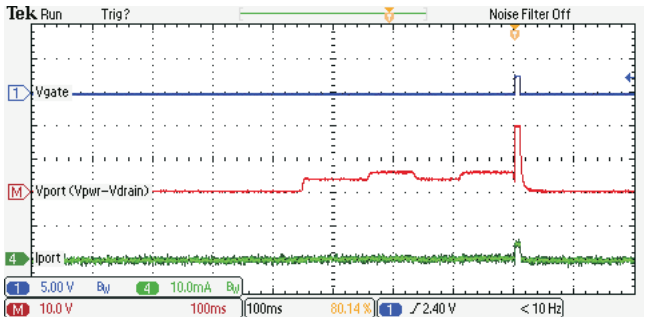


Figure 17. Valid PD Detection (25 kΩ and 0.1 µF) and CLASS 0 Classification

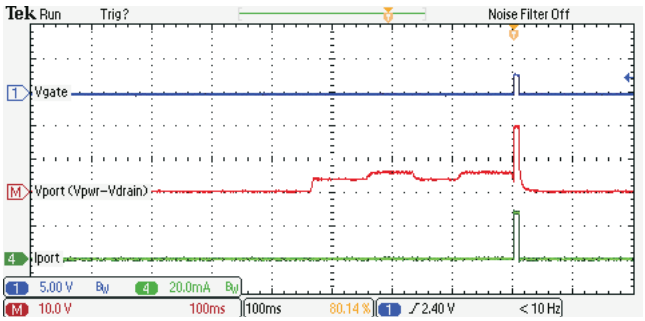


Figure 18. Valid PD Detection (25 kΩ and 0.1 µF) and CLASS 3 Classification

Typical Characteristics (continued)

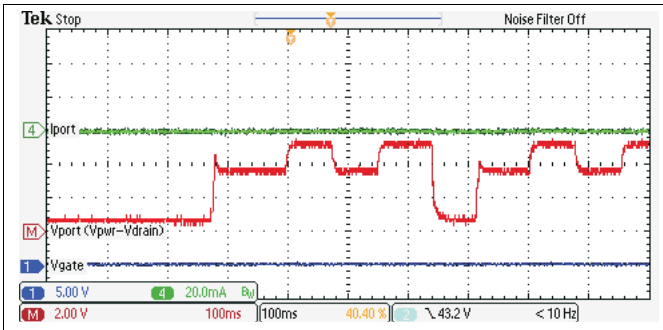


Figure 19. Detection with Invalid PD (15 kΩ and 0.1 µF)

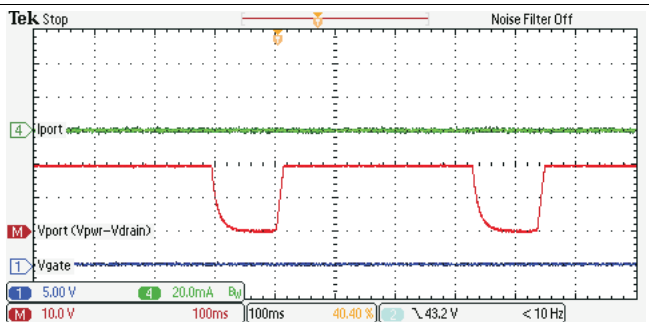


Figure 20. Detection with Invalid PD (open circuit)

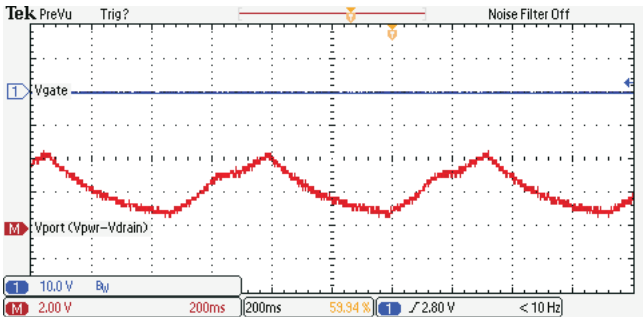


Figure 21. Detection with Invalid PD (25 kΩ and 10 µF)

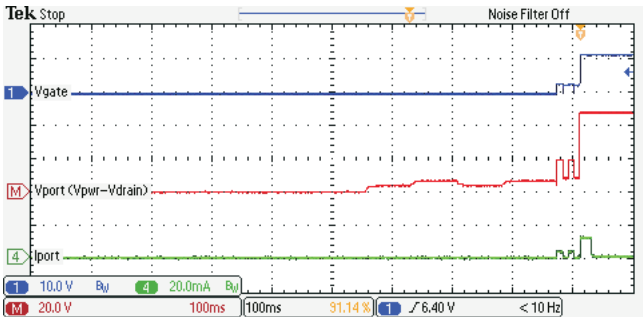


Figure 22. 2-Event Class and Startup with Valid PD

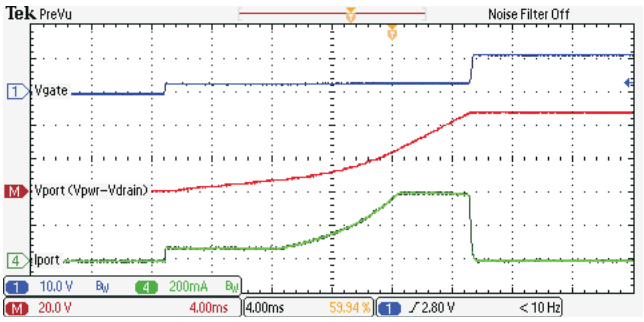


Figure 23. Powering Up Into a 100-µF Load

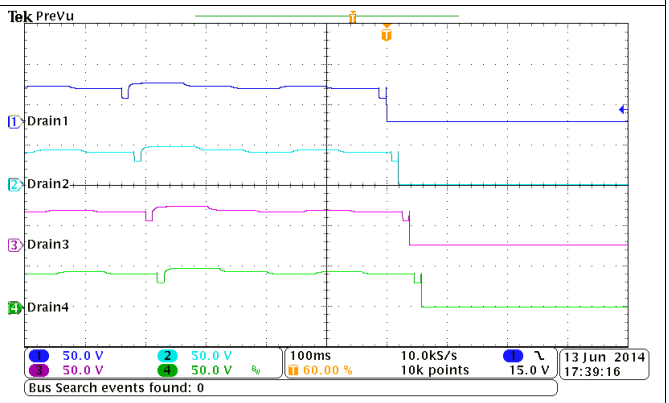


Figure 24. Semi-Auto Sequenced Turn On

Typical Characteristics (continued)

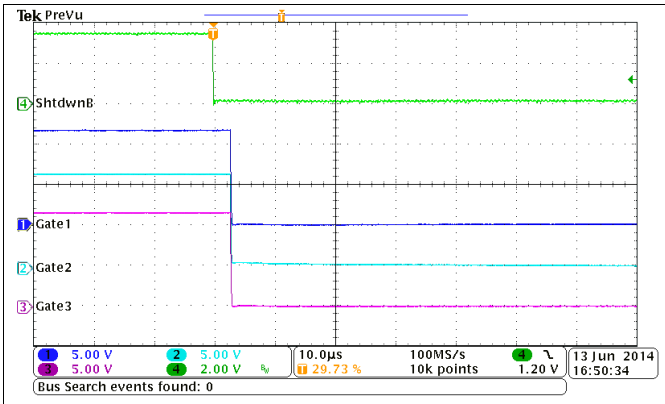


Figure 25. All Ports Fast Shutdown

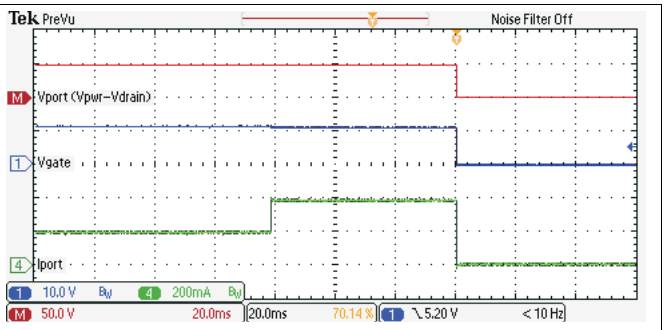


Figure 26. Overcurrent (I_{CUT}) Timeout

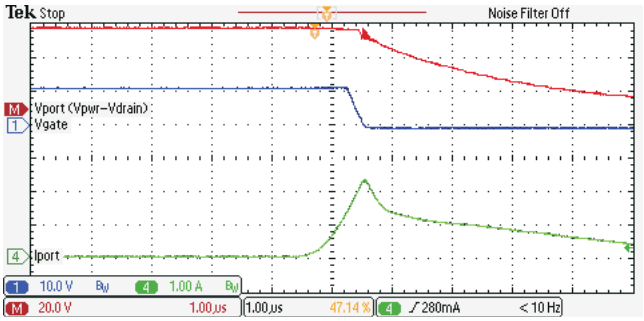


Figure 27. Rapid Response to a 1-Ω Short: 802.3af Mode

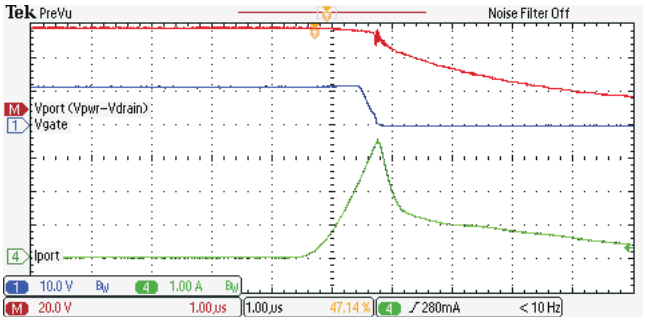


Figure 28. Rapid Response to a 1-Ω Short: PoE+ Mode

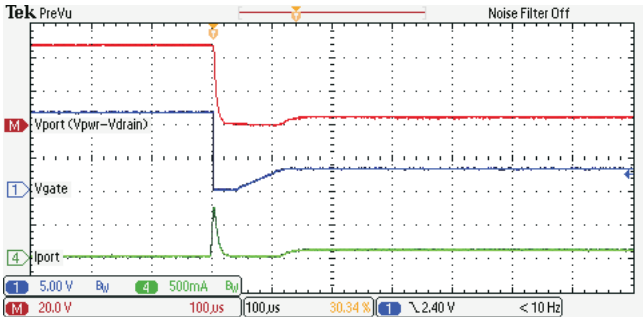


Figure 29. Response to a 50-Ω Load: 802.3af Mode

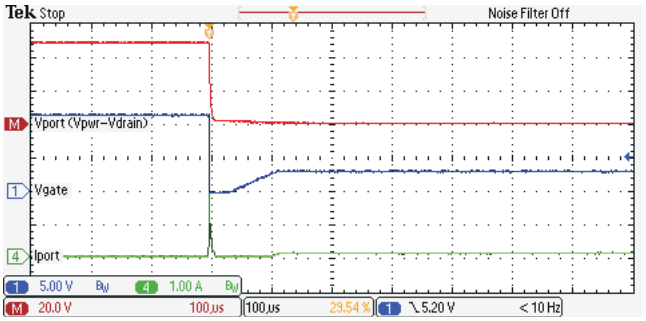


Figure 30. Response to a 25-Ω Load: PoE+ Mode

Typical Characteristics (continued)

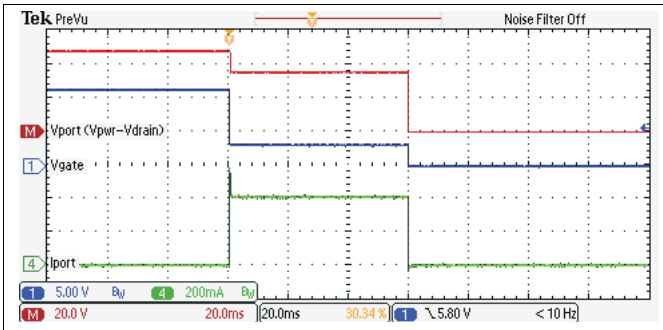


Figure 31. Current Limit Timeout: 802.3af Mode, 85-Ω Load

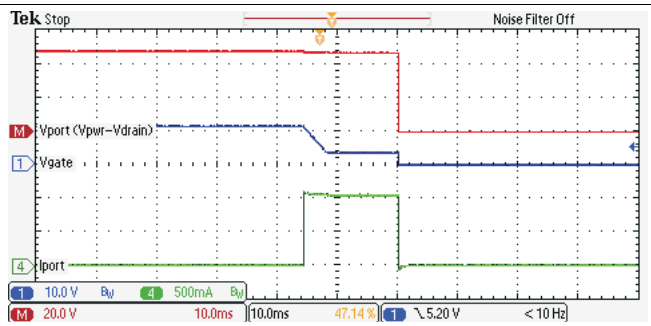


Figure 32. Current Limit 15-ms Timeout: PoE+ Mode, 45-Ω Load

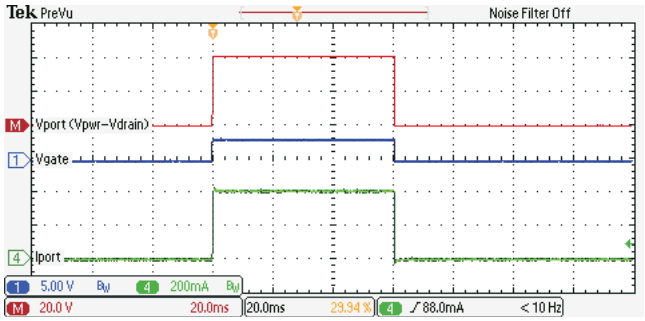


Figure 33. Inrush Fault Timeout: 100-Ω Load

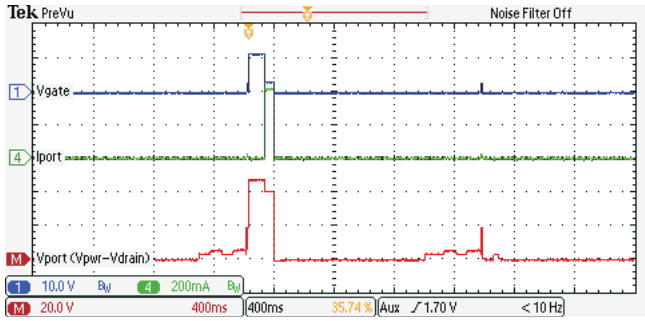


Figure 34. Current Limit Timeout Restart Delay

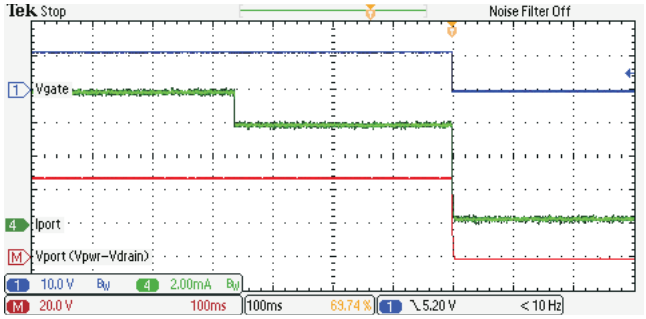


Figure 35. Response to 8-mA to 6-mA Load, DC Disconnect Enabled

7 Detailed Description

7.1 Overview

The TPS23861 is a four-port PSE for power over ethernet applications. Each of the four ports provides fully automatic detection, classification, protection, and shut down in compliance with the IEEE 802.3at standard.

The schematic of Figure 36 depicts automatic mode operation of the TPS23861, providing turnkey functionality ready to power PoE loads. No connection to the I^2C bus or any type of host control is required. In Figure 36 the TPS23861 automatically:

1. Performs four-point load detection.
2. Performs classification including type-2 (two-finger) of up to Class 4 loads.
3. Enables power with protective foldback current limiting, and ICUT value based on load class.
4. Shuts down in the event of fault loads and shorts.
5. Performs *Maintain Power Signature* function to ensure removal of power if load is disconnected.
6. Undervoltage lock out occurs if VPWR falls below V_{PUV_F} (typical 26.5 V).

Following a power-off command, disconnect or shutdown due to a start, ICUT or ILIM fault, the port powers down. Following port power off due to a power off command or disconnect, the TPS23861 will continue automatic operation starting with a detection cycle. If the shutdown is due to a start, ICUT or ILIM fault, the TPS23861 enters into a cool-down period. After the end of the cool-down period the TPS23861 continues automatic operation starting with a detection cycle.

The TPS23861 will not automatically apply power to a port under the following circumstances:

- The detect status is not Resistance Valid.
- If the classification status is overcurrent, class mismatch, or unknown.

Overview (continued)

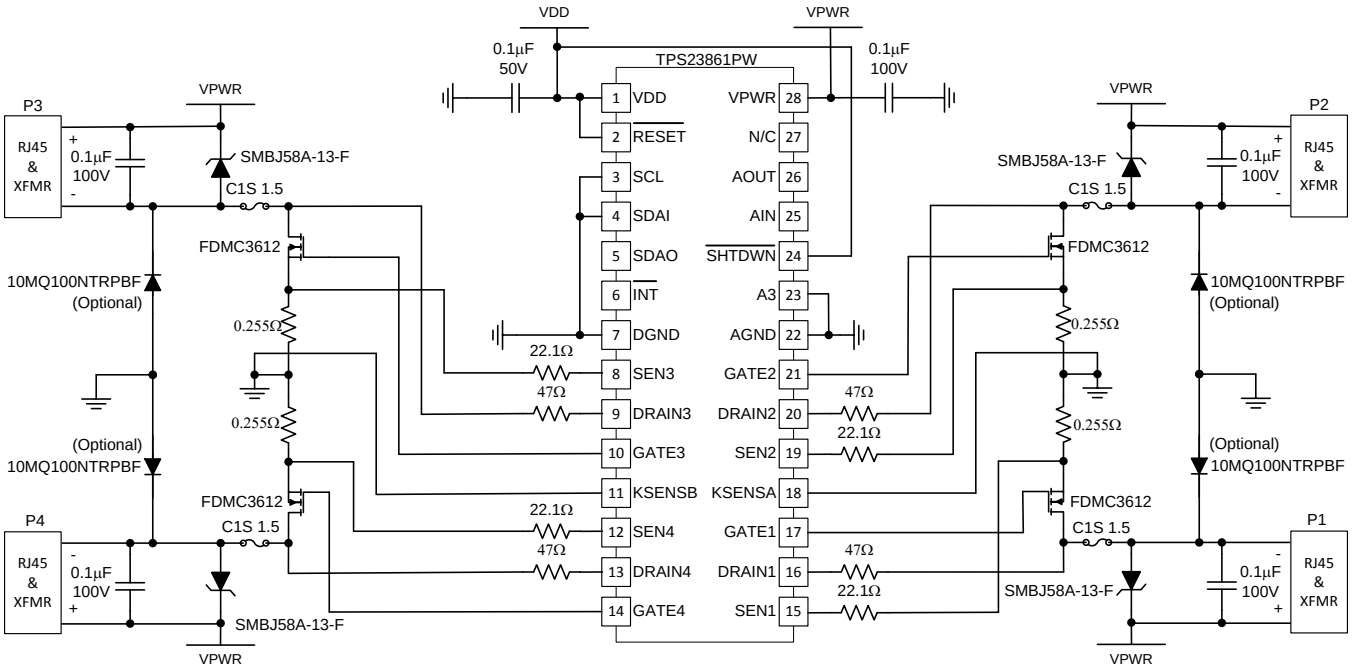


Figure 36. Automatic 4-Port Operation Schematic

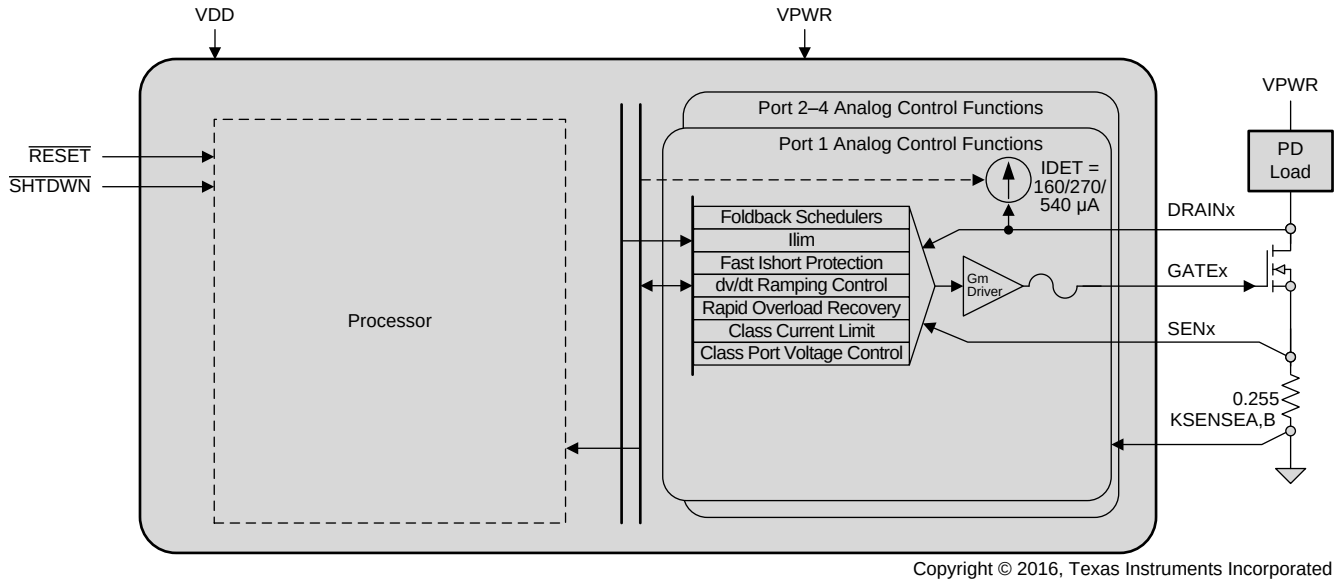


Figure 37. Simplified Block Diagram

Overview (continued)

7.1.1 Detailed Pin Description

The following descriptions refer to the pinout and the functional block diagram.

DRAIN1-DRAIN4: Port 1-4 output voltage monitor and detect sense. Used to measure the port output voltage, for port voltage monitoring, port-power-good detection and foldback action. Detection probe currents also flow into this pin. The TPS23861 uses an innovative 4-point technique in order to provide a reliable PD detection. Detection is performed by sinking two different current levels via the DRAINn pin, while the PD voltage is measured from VPWR to DRAINn. The 4-point measurement provides the capability to distinguish between an IEEE-standard-compliant PD and a capacitive or legacy load. If the Port n is not used, DRAINn can be left floating or tied to AGND.

GATE1-GATE4: Port 1-4 gate drive output used for external N-channel MOSFET gate control. At port turn on, it is driven positive by a low-current source to turn the MOSFET on. GATEn is pulled low whenever any of the input supplies are low or if an over-current timeout has occurred. GATEn will also be pulled low if its port is turned off during fast shutdown. Leave floating if unused. For a robust design, a current-foldback function limits the power dissipation of the MOSFET during low resistance load or a short-circuit event. The foldback mechanism measures the port voltage across AGND and DRAINn to reduce the current-limit threshold as shown in Figure 14, Figure 57, and Figure 58. The fast overload protection is for major faults like a direct short. This forces down the current within the current limit in less than a microsecond. When ICUT threshold is exceeded while a port is on, a timer starts. During that time, linear current limiting makes sure the current will not exceed ILIM combined with current-foldback action. When the timer reaches its t_{OVLD} (or t_{START} if at port turn on) limit, the port shuts off. When the port current goes below I_{CUT} , the counter counts down at a rate $1/16^{th}$ of the increment rate, and it must reach a count of zero before the port can be turned on again.

KSENSA, KSENSB: Kelvin point connection used to perform a differential voltage measurement across the associated current sense resistors. KSENSA is shared between SEN1 and SEN2, while KSENSB is shared between SEN3 and SEN4. In order to optimize the accuracy of the measurement, the PCB layout (see Figure 61) must be done carefully to minimize impact of PCB trace resistance.

$\overline{\text{SHTDWN}}$: Shutdown, active low. This pin is internally pulled up to VDD, with internal 1-µs to 5-µs deglitch filter. The Port Power Priority register is used to determine which port(s) is (are) shut down in response to an external assertion of the $\overline{\text{SHTDWN}}$ pin. The turn-off procedure is similar to a port reset or a reset command (Reset register).

NOTE

After a $\overline{\text{SHTDWN}}$ cycle occurs, the I^2C host should reinitialize the TPS23861 register set according to the desired user configuration. More detail regarding use of the $\overline{\text{SHTDWN}}$ pin to power off low priority ports can be obtained by consulting a Texas Instruments technical representative.

$\overline{\text{RESET}}$: Reset input, active low. When asserted, the TPS23861 resets, turning off all ports and forcing the registers to their power-up state. This pin is internally pulled up to VDD, with internal 1-µs to 5-µs deglitch filter. External RC network can be used to delay the turn-on. There is also an internal power-on-reset which is independent of the $\overline{\text{RESET}}$ input.

NOTE

After $\overline{\text{RESET}}$ pin de-assertion, there is a delay of approximately 20 ms before TPS23861 can process I^2C commands. For more information, refer to the application note TPS23861 Power-On Considerations, SLVA723.

Overview (continued)

SEN1- SEN4: Port 1-2 current sense input relative to KSENSA, and port 3-4 current sense relative to KSENSB. A differential measurement is performed using KSENSA and KSENSB Kelvin point connection. It monitors the external MOSFET current by use of either a 255-mΩ (two 510 mΩ in parallel) or a 250-mΩ (four 1 Ω in parallel) current-sense resistors connected to AGND. Used by current foldback engine and also during classification. Can be used to perform load current monitoring via A/D conversion.

NOTE

A classification is done while using the external MOSFET so performing a classification on more than one port at the same time is possible without exceeding dissipation in the TPS23861.

For the current limit with foldback function, there is an internal 2-µs analog filter on the SEN1-4 pins to provide glitch filtering. For measurements through an A/D converter, an anti-aliasing filter is present on the SEN1-4 pins. This includes the port-powered current monitoring and disconnect. If the port is not used, tie SENn to AGND.

VDD: 3.3-V logic power supply input.

VPWR: High-voltage power supply input. Nominally 48 V.

7.1.2 I^2C Detailed Pin Description

AIN: Used to program the I^2C slave device address. This pin is internally pulled up to VDD. See I^2C Slave Address and AUTO Bit Programming for more details.

AOUT: Used to program the I^2C slave device address for multiple devices. See I^2C Slave Address and AUTO Bit Programming for more details. AOUT is open drain.

A3: I^2C A3 address input, used during normal operation and during slave address programming. This pin is internally pulled up to VDD.

$\overline{\text{INT}}$: Interrupt output. This pin asserts low when a bit in the interrupt register is asserted. This pin is updated between I^2C transactions. This output is open-drain. Interrupt functional diagram is shown in Figure 43.

SCL: Serial clock input for I^2C bus. Requires an external pull-up resistor to VDD.

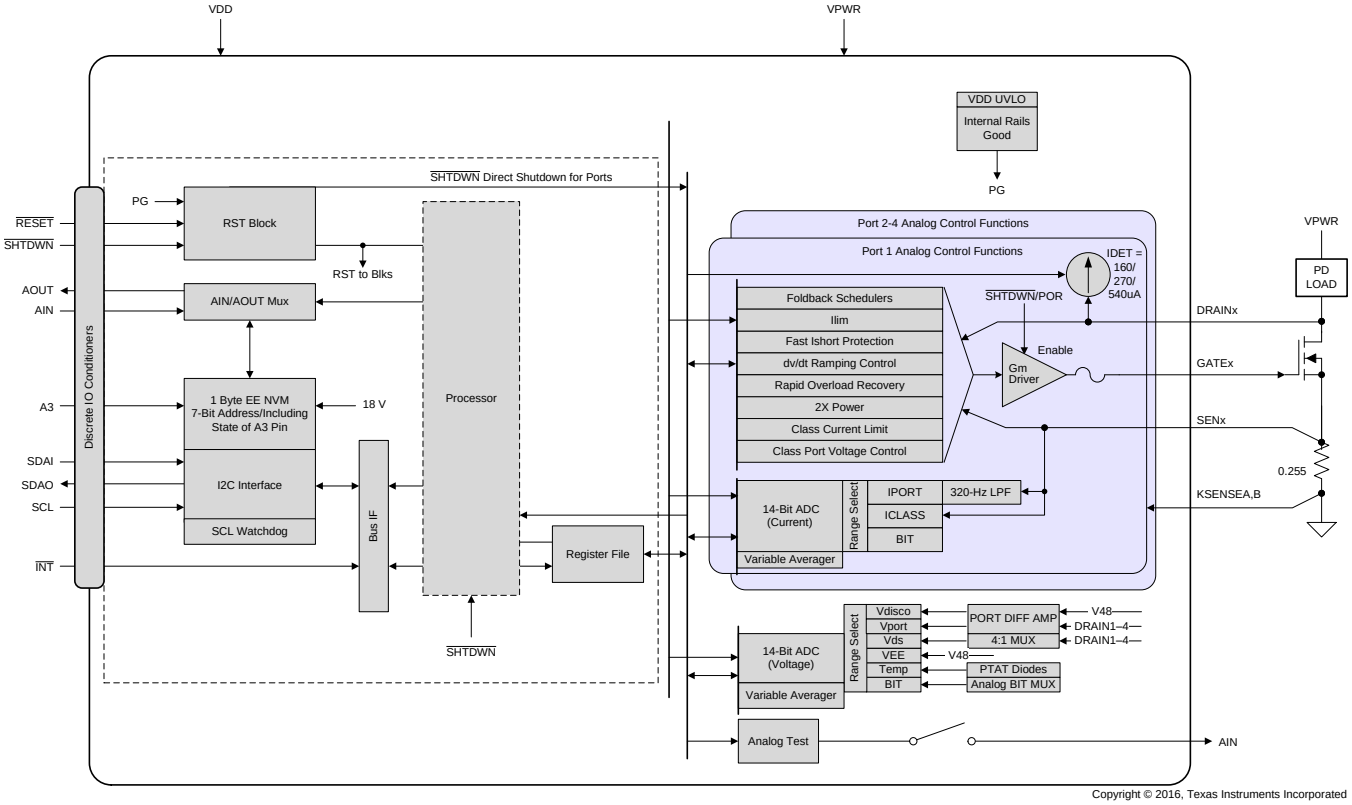
SDAI: Serial data input for I^2C bus. Requires an external pull-up resistor to VDD. This pin can be connected to SDAO for non-isolated systems. See Figure 50.

SDAO: Open-drain I^2C bus output data line. Requires an external resistive pull up. The TPS23861 uses separate SDAO and SDAI lines to allow optoisolated I^2C interface. SDAO can be connected to SDAI for non-isolated systems.

NOTE

Both VPWR and VDD must be present for proper system level I^2C operation.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Detection Resistance Measurement

The detect resistance can be measured and reported in the Port n Detect Resistance Register. Fourteen bits of resistance information are reported in two bytes. Useful range of measurement is 500 Ω to 55 kΩ. Resolution (1 LSB) is approximately 11 Ω. Measurement repeatability is on the order of ±200 Ω. Additionally, in the MSB of the resistance register (Port n Resistance: MSByte) the RSn field reports whether a low-resistance circuit, open circuit or MOSFET short fault is detected.

Before detection begins, the TPS23861 *backs-off* for up to 400 ms to allow the port voltage to drop below 2.8 V. This will allow any PD on the port to reset prior to an attempt to detect, classify and apply power to the PD.

Table 1. RSn Field Encoding

RSn1	RSn0	DETECT STATUS	R_{STEP} BIT WEIGHT
0	0	Other	11.0966 Ω/bit
0	1	Low (< 2 kΩ)	Additional detect 4.625 Ω/bit
1	0	Open circuit	N/A
1	1	MOSFET short fault	N/A

7.3.2 Physical Layer Classification

Whether one or two classification events will be executed depends on the operating mode and the value of the TECLENn field in the Two-Event Classification Register. See Device Functional Modes for details.

See Figure 38 and Figure 39 for illustrations of the voltage on the Power Interface (PI) during single-event (802.3af) and 2-event (802.3at) classification.

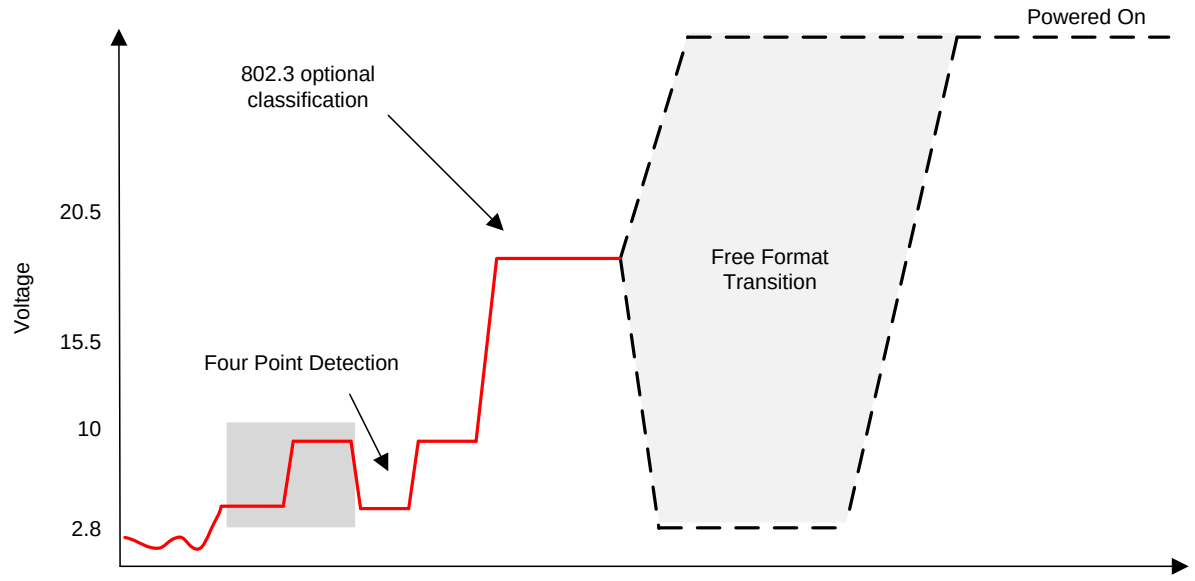


Figure 38. 802.3af with Classification

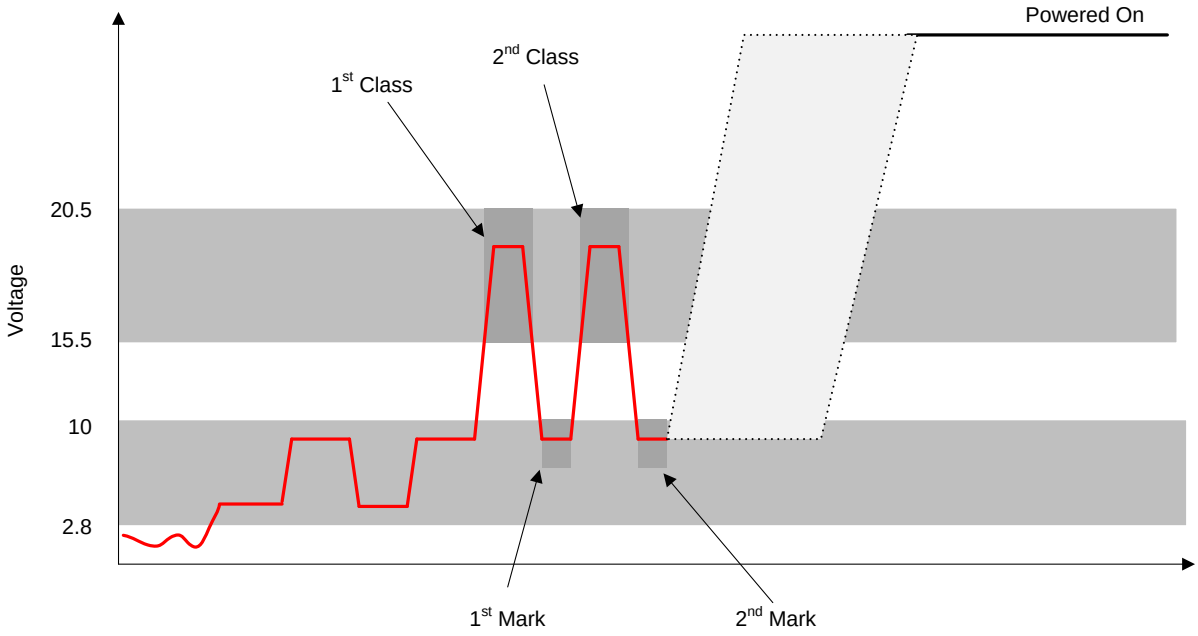


Figure 39. P802.3at with Classification

7.3.3 Class and Detect Fields

The results of the detection cycle and classification cycle are each stored in a 4-bit field for each port in the Detect Pn and Class Pn fields of the Port n Status Register. The results of a detection and classification event are encoded as follows.

Table 2. Detect Pn Field Encoding

DETECT Pn	DETECT STATUS
0000	Unknown (POR value)
0001	Short circuit (<500 Ω)
0010	Reserved
0011	Resistance too low
0100	Resistance valid
0101	Resistance too high
0110	Open circuit
0111	Reserved
1000	MOSFET fault
1001	Legacy detect
1010	Capacitance measurement invalid: Detect measurement beyond clamp voltage
1011	Capacitance measurement invalid: Insufficient Δv measured
1100	Capacitance measurement is valid, but outside the range of a legacy device.

Table 3. Class Pn Field Encoding

CLASS Pn	CLASSIFICATION STATUS
0000	Unknown
0001	Class 1
0010	Class 2
0011	Class 3
0100	Class 4
0101	Reserved – read as class 0
0110	Class 0
0111	Overcurrent
1000	Class mismatch

A class mismatch can occur only during two-event classification. If the classification statuses for the first and second event are different, and the second classification status is not “Overcurrent”, the Classification Status will be set to Class Mismatch. If the status of the first classification event is “Overcurrent”, the classification status is set to “Overcurrent” in the Class Pn field, and there will be no second classification event in any case. If in Auto Mode, the port will not power on automatically, but it still can be powered on through the Power Enable Register.

7.3.4 Register State Following a Fault

Following an ICUT, ILIM or inrush fault on port n, the port is shut off, and the appropriate fault bit is set in the Fault Event Register or Start/ILIM Event Register. In addition, the following registers are affected.

- The PGn and PEn in the Power Status Register are cleared.
- The CLSCn and DETCn bits in the Detection Event register are cleared.
- The corresponding Port n Status Registers are cleared.
- The PGCn and PECn bits in the Power Event Register are set.
- The PORT n Voltage Registers is cleared.

7.3.5 Disconnect

The TPS23861 supports DC disconnection. Disconnect threshold and timing are set using the DCTHn field in the Disconnect Threshold Register and the TDIS field in the Timing Configuration Register respectively. Following a disconnect event on port n, the following registers are affected.

- The DISFn bit in the Fault Event Register is set.
- The PGn and PEn in the Power Status Register are cleared.
- The CLSCn and DETCn status bits in the Detection Event Register are cleared.
- The corresponding Port n Status Registers are cleared.
- The PGCn and PECn bits in the Power Event Register are set.
- The corresponding Port n Voltage Registers are cleared.

7.3.6 Disconnect Threshold

The disconnect current range is selectable through the DCTHn 2-bit fields in the Disconnect Threshold Register. The encoding of the DCTHn fields is presented in Table 4.

Table 4. DCTHn Field Encoding

DCTHn FIELD	DISCONNECT THRESHOLD, mA
00	7.5
01	15
10	30
11	50

7.3.7 Fast Shutdown Mode

The TPS23861 responds to a low level on the $\overline{\text{SHTDWN}}$ pin by immediately turning off all ports preconfigured as *low priority* through the FSEn bits in the Port Power Priority Register. Reaction time is typically 2 µs. If an FSEn bit is set while the $\overline{\text{SHTDWN}}$ pin is low, the corresponding port is turned off and reset.

7.3.8 Legacy Device Detection

Legacy PDs which are not compliant with IEEE 802.3at can be identified on port n under control of the LEGMOD field in the Legacy Detect Mode Register. Two modes of legacy detection are supported. When LEGMODn = 10, port n is probed for IEEE 802.3at-based compliance (based on resistance measurement) followed by a capacitance-based detection scheme for legacy devices. When LEGMODn= 01, port n performs a capacitance-based detection scheme only. This allows the host to probe for a potential legacy PD without pre-charging the PD capacitance before trying to measure the value of the capacitance.

To measure capacitance, a fixed charge is injected into the Power Interface (PI) and the voltage difference induced by the charge is measured and reported in the Port n Detect Voltage Difference Registers. The capacitance is inversely proportional to the voltage difference. The voltage difference is compared against thresholds to accept capacitance values above 6 µF pursuant to the qualifications which follow.

The Port n Detect Voltage Difference Register consists of two contiguous bytes in the I^2C addressable register space. Together these registers contain a 12-bit unsigned representation of the voltage difference along with a 4-bit status field named VDSn. When VDSn = 0001 the voltage-difference value represents a valid measurement. The capacitance measurement may fail due to an excessively small or large capacitance, or an input capacitance which cannot be discharged because it is behind a diode. These cases are reported in the VDSn field as well as in the DETECT Pn field in the Port n Status Registers. See Table 5.

Table 5. Capacitance Measurement Characteristics and Capabilities

PARAMETER	CONDITIONS	VALUE	UNIT
Minimum measurable capacitance	Maximum 500-kΩ parallel resistance; maximum measurement voltage of 16.5 V at port	6.1	µF
Maximum measurable capacitance	Minimum 17-kΩ parallel resistance	100	µF
Maximum measurable capacitance	Minimum 10-kΩ parallel resistance	67	µF
Nominal port charging current		540	µA
Nominal measurement time		150	ms
Minimum voltage at port for commencement of measurement		0.4	V
Maximum voltage at port for commencement of measurement		2.4	V
Duration of port-discharge period	First discharge attempt	250	ms
Duration of port-discharge period	Second discharge attempt	500	ms
Maximum voltage at port at the beginning or end of measurement		16.5	V

A resistance in parallel with the capacitance at the input of the PD affects the accuracy of the capacitance-measurement algorithm. A parallel resistance causes the capacitance on the port to appear higher. This fact is reflected in Table 5 . Capacitance up to 100 µF can be measured with a parallel resistance as low as 17 kΩ, whereas if the parallel resistance is as low as 10-kΩ, capacitance up to 67 µF can be measured.

The voltage on the port must be in the range of 0.4 V to 2.4 V to begin capacitance measurement. This voltage as measured at the PSE includes the voltage drops across any diodes in the path of the capacitance. If the voltage measured is too high (due to charge on the PD capacitance), the TPS23861 makes two attempts to discharge the port by applying a 100-kΩ load across the port. The first discharge attempt is 250-ms duration; the second attempt 500 ms.

NOTE

It may not be possible to discharge the PD capacitance rapidly if the capacitance is on the other side of a diode.

If the capacitance-measurement algorithm is unable to discharge the port to less than 2.4 V after two attempts, the algorithm terminates the attempt to measure port capacitance, and report an *Unable to achieve 2.4 V to take first measurement* status in the VDSn field of the Port n Detect Voltage Difference Registers. A status of *Capacitance measurement invalid: Insufficient Δv measured* is reported in the Port n Status Registers. A status of *Unable to discharge PD input capacitance to 2.4 V before timeout*, is reported in the VDSn field of the Port n Detect Voltage Difference Registers. The host has the option of imposing a longer discharge time and retrying.

Erratic results may be obtained when performing legacy detect in Semi-Auto Mode due to the repeated charging of the load. If the capacitive load is behind a diode or is in parallel with a high resistance, the capacitor may eventually charge beyond 2.4 V, and the capacitance measurement fails. Manual Mode is recommended for legacy detect when there is no information about the load, or if the load input capacitance charges beyond 2.4 V in Semi-Auto Mode.

If the port is open or a small capacitance is present on the port, the port voltage rises quickly when the capacitance-measuring current is applied. The voltage on the port is limited to approximately 18 V by an internal clamp. A status of *Capacitance measurement invalid: Detect measurement beyond clamp voltage* is reported in the DETECT Pn field of the Port n Status Registers. Depending on the size of the small capacitance, a status of *First measurement exceeds* $V_{Det\text{-}clamp\ (min)}$ or *Second measurement exceeds* $V_{Det\text{-}clamp\ (min)}$ is reported in the VDSn field of the PORT n Detect Voltage Difference Registers.

If a large capacitance or short circuit is present on the port, the port voltage will not change sufficiently over the port charging time to assure a reliable measurement. In this case, a status of *Capacitance measurement invalid: Insufficient Δv measured* is reported in the Port n Status Registers, and a status of *Δv < 0.5 V (insufficient signal)* or *Unable to achieve 0.4V to take first measurement before timeout* is reported in the VDSn field of the Port n Detect Voltage Difference Registers.

Legacy detect is an exceptional condition which warrants special handling by the host system. Consequently, legacy-detect operation will not be fully supported in Auto Mode. If a legacy device is detected during detection in any mode of operation, the detect status is reported as Legacy Detect in the Port n Status Register Detect Pn field. It is up to the host to power on the port. If a port is in Auto Mode, legacy detection is enabled and a legacy device is detected, the detect status is reported as Legacy Detect in the Port n Status Registers Detect Pn field, but the port will not power on automatically. In this respect, operation of the port is identical to the Semi-Auto Mode.

In general, it is expected that a legacy device will not respond to a request for classification. Therefore, if the port is in Semi-Auto or Auto Mode and detect status is Legacy Detect, the PSE will not automatically initiate a classification cycle even if the CLEn bit is set. On the other hand, if LEGMOD = 10, the TPS23861 is operating in Semi-Auto or Auto Mode, classification is enabled via the CLEn bit, and a Resistance valid detect status is returned in response to a standard resistance detection cycle, the TPS23861 follows the standard resistance detection cycle with a classification cycle. Furthermore, following classification, if in Auto Mode, if the classification status is not unknown, class mismatch or overcurrent, the port automatically powers up. It is possible to initiate a classification cycle under manual control using the CLEn bit in the Detect/Class Enable Register or the RCLn bit in the Detect/Class Restart Register or power on the port under manual control using the PWONn bit in the Power Enable Register.

If LEGMODn = 10, and a Resistance valid detect status is returned in response to a standard resistance detection cycle the TPS23861 will not attempt to measure capacitance on the PI.

7.3.9 VPWR Undervoltage and UVLO Events

This section lists the behavior of VPWR undervoltage and UVLO events when the voltage at the VDD pin is uninterrupted.

When the voltage at the VPWR pin falls below V_{PUV_F} the following occurs.

- The VPUV bit in the Supply Event Register is set.
- All ports are shut off.
- For ports that are shut off the corresponding PGCn and PECn bits in the Power Event Register is set and the PGn and PEn bits in the Power Status Register are cleared.
- The following registers are cleared.
  - Detection Event Register
  - Fault Event Register
  - Start/ILIM Event Register
  - Port n Status Register
  - Detect/Class Enable Register

NOTE

When the voltage at the VPWR pin falls below V_{UVLOPW_F} the following occurs.

- Both the VPUV and VDUV bits in the Supply Event Register is set
- All ports are shut off
- All registers are set to their power-on/reset state

7.3.10 Timer-Deferrable Interrupt Support

A programmable timer is provided with range selectable from 10 ms to 150 ms in 10 ms increments. Timer duration is programmed via the four-bit field TMR [3:0] in the Interrupt Timer Register. Non-critical interrupts will be deferred from asserting an interrupt on the $\overline{\text{INT}}$ pin until the timer times out. Critical interrupts such as faults will not be affected by the state of this timer. Critical vs. deferrable interrupts are identified in Table 6. The behavior of the various interrupt enable bits is not affected by the timer function.

Table 6. Timer-Deferrable Interrupt

INTERRUPT BIT	FUNCTION	CRITICAL OR DEFERRABLE
SUPF	Supply or thermal fault	Critical
STRTF	Start fault	Deferrable
IFAULT	ICUT or ILIM fault	Critical
CLASC	A classification event occurred	Deferrable
DETC	A detection event occurred	Deferrable
DISF	A disconnect event occurred	Deferrable
PGC	Power good status change	Deferrable
PEC	Power enable status change	Deferrable

If the counter is loaded with 0000 (POR state) the counter will not count, and no interrupts will be deferred. That is, this function will be disabled.

7.3.11 A/D Converter and I²C Interface

The TPS23861 features five multi-slope integrating converters. Each of the first four converters is dedicated to current measurement for one port and is operated independently to perform measurements. The converters are used for current monitoring (100 ms averaged) and disconnect. The fifth converter is shared between all four ports for detection (conversion time set by MAINS bit), port voltage monitoring, Power Good Status and FET short detection (1 ms for all). It is also used for general-purpose measurements including input voltage (1 ms) and temperature.

The A/D converter type used in the TPS23861 differs from other types of converters in that it converts while the input signal is being sampled by the integrator, resulting in reduced conversion time and providing inherent filtering over the conversion period. The typical conversion time of the current converters is 800 µs. Digital averaging is used to provide a port current measurement integrated over a 100-ms time period.

NOTE

An anti-aliasing filter is present for current and voltage monitoring. Port current conversions are performed continuously.

Powered device (PD) detection is performed by averaging 16 consecutive samples providing significant rejection of noise at 50/60-Hz line frequency. The total time for the 16 samples can be set to 20 ms or 16.7 ms by the MAINS bit to correspond to the local mains frequency.

The fifth converter continuously measures drain voltages from one port to the next one, updating internal registers used for Power Good Status and FET short detection, unless a command is received to perform a specific measurement.

Also, when the port is powered on, the t_{START} timer (used during PD power-on inrush) must expire before any current or voltage A/D conversion can begin for the first four converters.

Figure 40 illustrates read and write operations through I²C interface. The two-data-bytes-read operation is applicable to A/D conversion results.

It is also possible to perform an I²C write operation to many TPS23861 devices at same time. The slave address during this broadcast access is 0x30.

The TPS23861, using the $\overline{INT}$ pin, supports the SMBALERT protocol. When $\overline{INT}$ is asserted low, if the bus master controller sends the alert response address, the TPS23861 responds providing its device address on the SDA line and releases the $\overline{INT}$ line. If there is a collision between two TPS23861 devices responding simultaneously, then the device with the lower address wins arbitration and responds first, by use of SDAI and SDAO lines.

An I²C watchdog timer is also available on the TPS23861, which monitors the I²C clock line in order to prevent hung software situations that could leave ports in a hazardous state. The timer can be reset by either edge on the SCL line. When enabled, if the watchdog timer expires, all ports are turned off and WDS bit is set. The nominal watchdog time-out period is 2 seconds. See I²C Watchdog Register for more details on the subject.

NOTE

When a stop condition is detected on the I²C bus after having at least received the command byte, the TPS23861 stores the command byte in an internal register.

NOTE

When using the I²C interface the host software should wait 22 ms minimum after a reset to ensure valid I²C transactions.

This content can be later used as a register address pointer during next *quick read cycle* register access. See Figure 40. This internal register is cleared at power on or through the RESET pin.

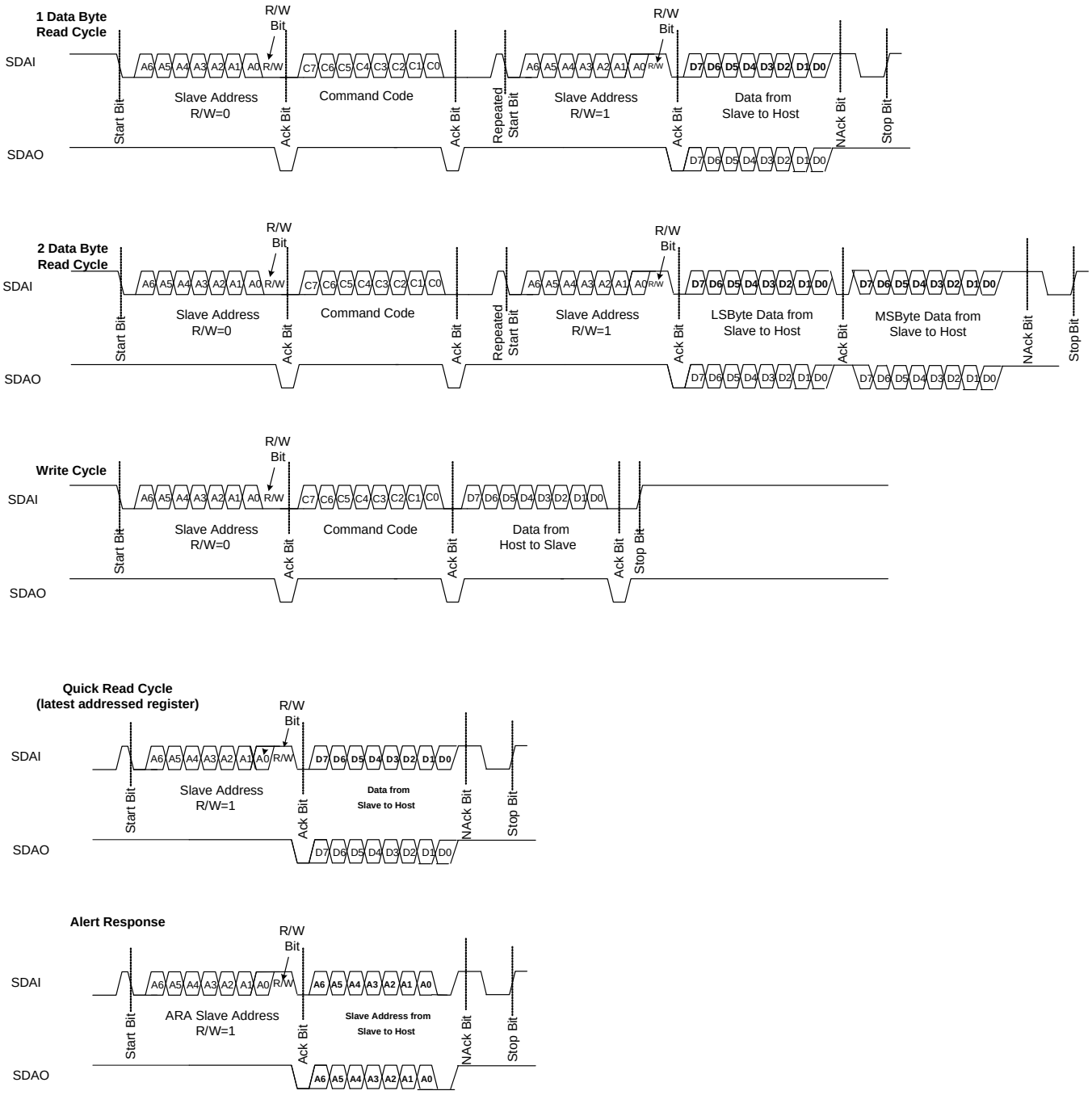


Figure 40. I²C/SMBus Interface Read and Write Protocol

7.3.12 Independent Operation when the Bit is Set

The TPS23861 operates as a fully automatic PSE in compliance with IEEE 802.3at when the AUTO bit is set as described in I²C Slave Address and AUTO Bit Programming section. Fully automatic operation means that the TPS23861 operates as a power-over-ethernet four-port PSE without any connection to a host system via the I²C bus. Generally speaking, when the bit is set, most specialized features of the TPS23861 are disabled.

NOTE

The state of the AUTO bit is read only following power on, hardware reset ($\overline{\text{RESET}}$ pin) or writing a 1 to the RESAL bit in the Reset Register.

If the AUTO bit is set and the TPS23861 is connected to a host over the I²C bus, the host may change the register settings any time after power up, including changing operating mode. When the AUTO bit is set, the state of TPS23861 following power up is summarized below.

- The CLEn and DETn bits in the Detect/Class Enable Register is set. Consequently, detect and classification is performed before any power on.
- The DCDEn bit in the Disconnect Enable Register is set, enabling automatic disconnection.
- The TECLENn bits in the Two-Event Classification Register is set to 0b01. Consequently, if a Class 4 PD is recognized during the classification cycle,
  - The TPS23861 initiates a second physical-layer classification event.
  - The PoEPn bit in the PoE Plus register is set, employing the 2x curve for I_{LIM}.
  - The ICUT Port n fields in the ICUTnm CONFIG registers will be set to 0b110 corresponding to 645 mA.
- If a Class 0, 1, 2 or 3 PD is recognized during the classification cycle,
  - There is no second physical-layer classification event.
  - The POEPn bit is cleared so the TPS23861 employs the 1x foldback curve for I_{LIM}.
  - A value of 374 mA is used for ICUT.
- The Port n Mode field in the Operating Mode Register is set to Auto (0×11) for all four ports. Consequently,
  - Detection, classification and power up occurs in sequence, automatically and independently for each port.
  - Following a valid one- or two-event physical layer classification, the TPS23861 applies power to a port subject to the inrush-current foldback protection curve in Figure 57.

  .
- The FSEn bits in the Port Power Priority Register is set. Consequently, all ports are shut down in response to a low level on the $\overline{\text{SHTDWN}}$ pin.
- The LEGMODn fields in the Legacy Detect Mode Register is set to 00. Consequently, legacy PD devices not compliant with IEEE 802.3at will not be detected.
- The General Mask 1 Register is set to its standard power-on-reset value 0x80. Consequently,
  - Interrupts are enabled.
  - During detection A/D conversions of the detect voltage occurs at a rate of 800 per second.
  - Classification levels are determined as if a 255-mΩ resistor is used for the current-sense resistor.

NOTE

If a 250-mΩ resistor is used, the classification thresholds shifts slightly, but remains compliant with IEEE 802.3at.

- The Interrupt Enable Register is set to 0xE4, enabling the following interrupts
  - SUPEN – Supply event fault enable bit.
  - STRTEN – Start fault enable bit.
  - IFEN – ICUT or ILIM fault enable bit.
  - DISEN – Disconnect event interrupt enable bit.
- Any register not explicitly referenced above is set to its default power-on-reset value according to Table 10.

7.3.13 I²C Slave Address and AUTO Bit Programming

NOTE

When using the I²C interface the host software should wait 22 ms minimum after a reset to ensure valid I²C transactions.

NOTE

Please note EEPROM endurance of 25 write cycles. Writing to the EEPROM more than this may result in erratic behavior.

The TPS23861 includes a means to program in EEPROM the following two fields:

- A seven bit I²C slave address for operation with a host processor.
- AUTO bit which allows the TPS23861 to operate independently without a host processor.

The benefits this approach include:

- Up to 125 similar devices become addressable.
- Provides a high level of flexibility.
  - Helps to resolve conflicts with other peripherals on same I²C bus.
  - The I²C address can be programmed at production subassembly module level or motherboard level.
  - Allows a simple approach to field-installed upgrades or expansions to PSE systems.
- No physical address line required, no bank selection required.
- Smaller package. No address line pins and no AUTO pin.

NOTE

For compatibility with legacy systems, the *module A3 bank addressing* is provided by use of the A3 input pin.

As shown in Figure 41, the initial I²C address programming access is established by a local daisy chain *chip select* connection between multiple TPS23861 devices. The AIN pin plays the role of a “moving chip select” during address programming.

NOTE

Global write command including an unlock code (AAh) is required in order to write to the I²C slave address register.

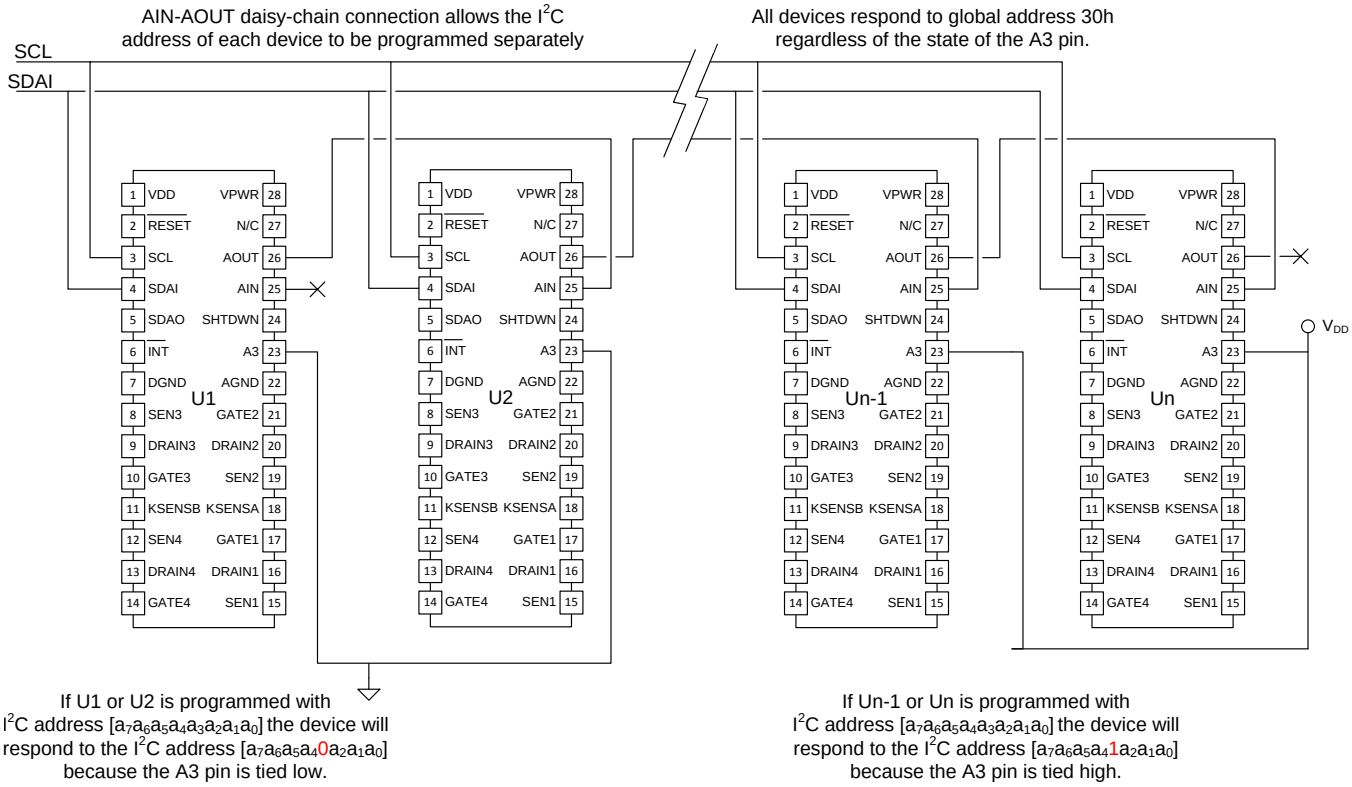


Figure 41. I²C Slave Address and AUTO Bit Programming Circuit

The sequence during address programming is as follows:

- Global write command including an unlock code (AAh) and a temporary common slave address (any address other than 30h) is sent to all I^2C devices through the broadcast address, 30h.
- All TPS23861 devices respond to the broadcast address 30h regardless of the state of the A3 pin. When the three-byte sequence is correctly decoded,
  1. Each TPS23861 has a new I^2C address determined by the programmed temporary slave address with bit 3 equal to the state of the A3 pin.
  2. All TPS23861 devices force low the AOUT output.

  For example, if a temporary common slave address of 20h is written to one device with A3 low and one with A3 high, the device with A3 low will respond to I^2C address 20h and the device with A3 high responds to I^2C address 28h.
- The first TPS23861 device being selected is the only one having its AIN pin at logic high level (U1 in Figure 41).
- Using the temporary slave address, write the new 7-bit device address in the I^2C slave address register. See data format below.

NOTE

The SLA3 slave address bit follows the logic level of A3 input pin, as detailed for I^2C Slave Address register.

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	AUTO	7-bit I^2C Address						

- The first slave accepts the new address, then forces its AOUT output pin to high level and automatically locks the access to its slave address register. It also stores permanently its new slave address into EEPROM.
- The same procedure is repeated for the next slave device, which has just detected that its AIN input has become high.
- This is repeated until all slaves have been reprogrammed.
- The host can then interrogate each slave, one by one, in order to validate their new address.

NOTE

During the address programming procedure if the slave has not received its new address within a timeout period (around 100 ms), it goes back to the initial slave address (before the address programming sequence was initiated); it locks its address register and releases its AOUT output.

- Bit 7 of the 8-bit transfer (AUTO) defines if the controller operates independently (no host processor) as an automatic PSE. The state of this bit is monitored only immediately following a power-on reset, writing a 1 to the RESAL bit of the RESET register, or after the $\overline{\text{RESET}}$ input has been activated. The impact of that bit state on registers after reset is reflected in the Table 10 (Reset State column) and is referred to as “A”.

NOTE

After programming a new I^2C slave address to register 0×11, a 100 ms delay is recommended before trying to perform a read check.

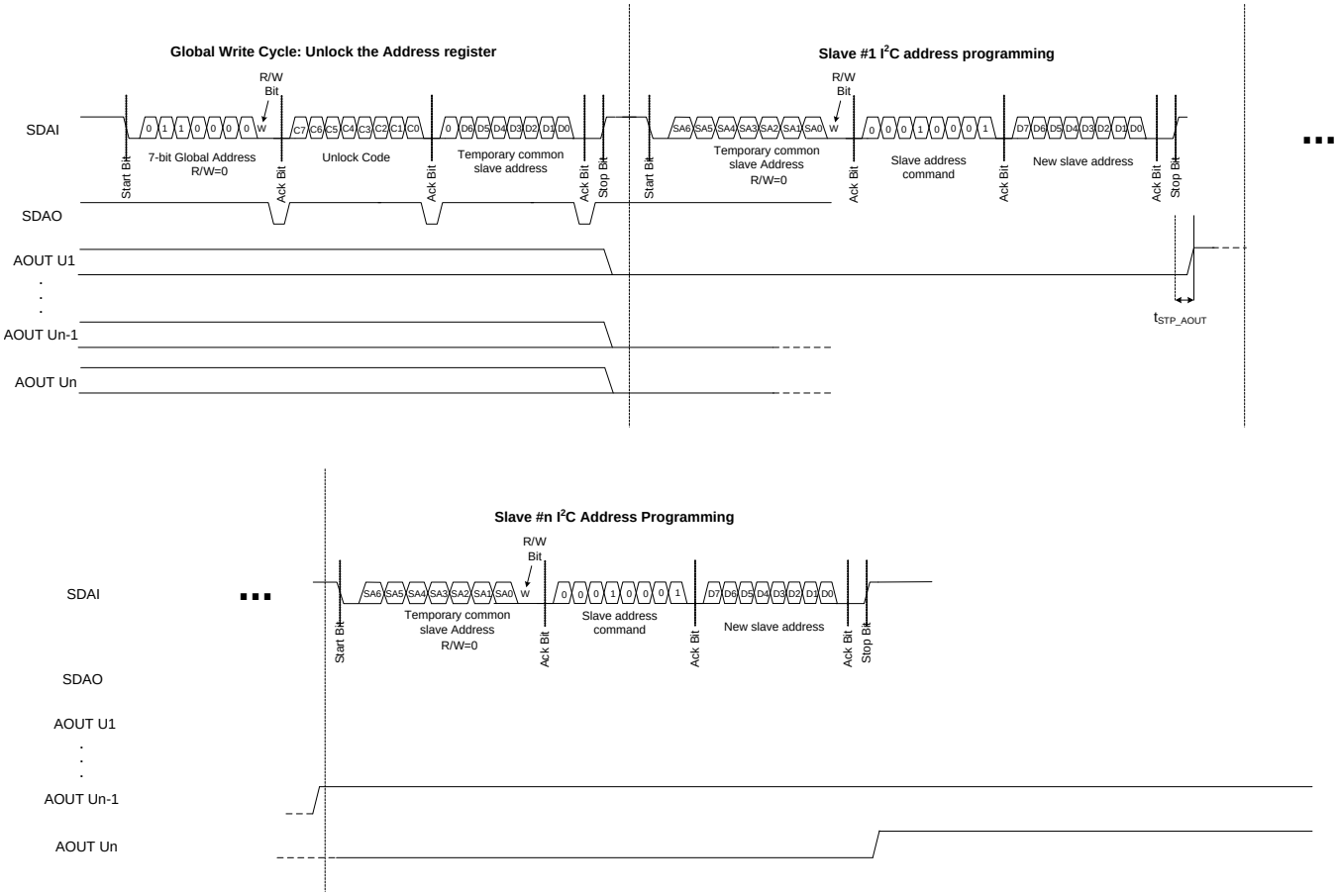


Figure 42. I²C/SMBus Interface Slave Address Programming Protocol

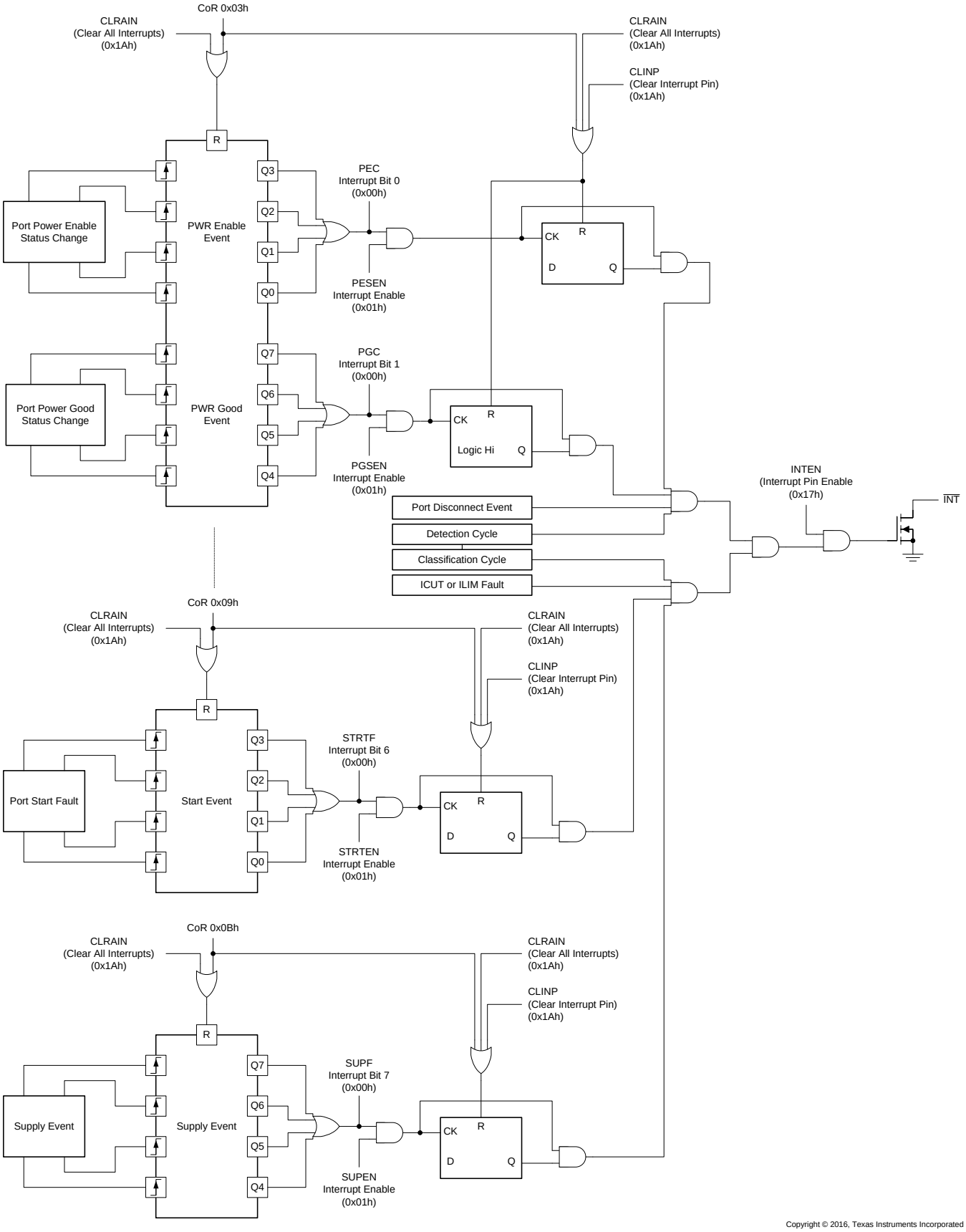


Figure 43. Interrupt Logic Functional Diagram

7.4 Device Functional Modes

Four operating modes are defined as follows. Operating mode is controlled for each port through the Port n Mode field in the Operating Mode Register. Operating mode codes appear in Operating Mode Register.

7.4.1 Off

Port n will not detect, classify or power on. When the operating mode of port n is set to Off the following takes place.

- Port voltage and current are monitored continuously. The results are reported in the Port n Voltage and Port n Current Registers.
- The CLSCn and the DETCn bits in the Detection Event register are cleared.
- The Port n Status register is cleared.
- The CLEn and the DETEn bits in the Detect/Class Enable register are cleared.
- The DISFn and the ICUTn bits in the Fault Event Register are cleared.
- The ILIMn and STRTn bits in the Start/ILIM Event register are cleared.
- If the port was powered on when the operating mode is set to Off, the port is shut off, and the following occurs.
  - The PGCn and the PECn bits in the Power Event Register are set.
  - The PGn and PEn bits in the Power Status register are cleared.

7.4.2 Manual

NOTE

In order to meet the IEEE 802.3at standard, PWONn bit should be set within 22 ms after classification is completed if two-event classification is applied.

There is no automatic change of state. A single detection or classification event may be initiated by writing to the appropriate bit of the Detect/Class Restart Register which is a pushbutton register. Furthermore, setting the DETEn bit initiates one detect cycle for Port n; setting the CLEn bit initiates one classify cycle for Port n. The number of classification events depend on the classification status of the first classification event and the setting of the TECLENn field as shown in Table 7.

Table 7. Number of Classification Events in Manual Mode

CLASSIFICATION STATUS OF FIRST CLASSIFICATION EVENT	VALUE OF TECLENn	TOTAL NUMBER OF CLASSIFICATION EVENTS
Class 0, Class 1, Class 2 or Class 3	XX	One
Class 4	X0	One
	X1	Two

In manual mode, writing to the pushbutton PWONn bit powers on Port n immediately.

NOTE

In Manual mode, the ICUTn and PoEPn fields are not set automatically. They must be set by the host. Furthermore, there is no cool-down period in manual mode.

7.4.3 Semi-Auto

No activity takes place on the port until the DETEn bit in the Detect/Class Enable register is set. When DETEn is set, port n automatically performs detection. If a valid PD is detected and CLEn is set, the port initiates a classification cycle. The classification cycle is single-event if a class 0, 1, 2 or 3 PD is recognized. If the first classification event returns a class 4 signature, a second classification event is initiated depending on the setting of the TECLENn field in the Two-Event Classification Register. The cycle of detect, then classification repeats continuously.

Powering on the port requires writing to the pushbutton PWONn bit in the Power Enable Register. The port powers on meeting the IEEE $T_{P(on)}$ requirement to power on within 400 ms of the end of a valid detection. Depending on the timing of the PWONn command, the controller may initiate a new detect and (if CLEn is set) classification sequence before powering on the port if required to meet the $T_{P(on)}$ requirement. If the final detect is invalid, or if the final classification returns overcurrent or class mismatch, the port will not power on and the STRTn bit is set in the Start/ILIM Event Register. For Turn-On sequencing see Push-Button Power On Response.

NOTE

In Semi-Auto Mode, the ICUTn and PoEPn fields are not set automatically. They must be set by the host.

Following a power-off command, disconnect or shutdown due to a Start, ICUT or ILIM fault, the port powers off. Following a shutdown due to a start, ILIM or ICUT fault, the TPS23861 enters into a cool-down period. During the cool-down period any port power on command using Power Enable Command is ignored. The length of the cool-down period is set in the CLDN field of the Cool Down/Gate Drive Register. After the end of the cool-down period the TPS23861 initiates a detect cycle and continues semi-automatic operation.

NOTE

TI recommends using this reference code to develop your software

http://www.ti.com/product/TPS23861/toolssoftware

7.4.4 Auto

In Auto Mode the TPS23861 automatically cycles the port through detection, classification and power on. The ICUT and PoEP fields are set automatically based on the classification status. If a class 0, 1, 2 or 3 PD is recognized, ICUTn is set to 000 (374 mA) and the PoEPn bit is cleared. If a class 4 PD is recognized, ICUTn is set to 110 (645 mA) and the PoEPn bit is set. Auto Mode and the AUTO bit are related, but are not identical. When the Bit is set, all ports are placed in Auto Mode; additionally, several other registers are set. See Independent Operation when the Bit is Set section.

Following a power-off command, disconnect or shutdown due to a Start, ICUT or ILIM fault, the port powers off. Following port power off due to a power off command or disconnect, the TPS23861 continues automatic operation starting with a detection cycle (if DETEn is set). If the shutdown is due to a Start, ICUT or ILIM fault, the TPS23861 enters into a cool-down period. During the cool-down period any port power-on command using Power Enable Command is ignored. The length of the cool-down period is set in the CLDN field of the Cool Down/Gate Drive Register. After the end of the cool-down period the TPS23861 continues automatic operation starting with a detection cycle, assuming DETEn is set.

The TPS23861 will not automatically apply power to a port, even if Operating Mode is set to Auto, under the following circumstances.

- The detect status is not Resistance Valid. This means that the DETEn bit must be set in order to power on in Auto Mode.

NOTE

A write to the DETEn bit or CLEn bit will not *stick* if the port is in Off Mode.

- If the classification status is overcurrent, class mismatch or unknown.

The TPS23861 starts in Auto Mode after a power-on reset or when the RESET pin is de-asserted. When a valid PD is connected as TPS23861 comes out of reset, then the ports will sequence through detection, classification, and power on as shown in Figure 44. Staggered port power on prevents the sudden inrush of current from the VPWR supply when multiple PDs are already connected.

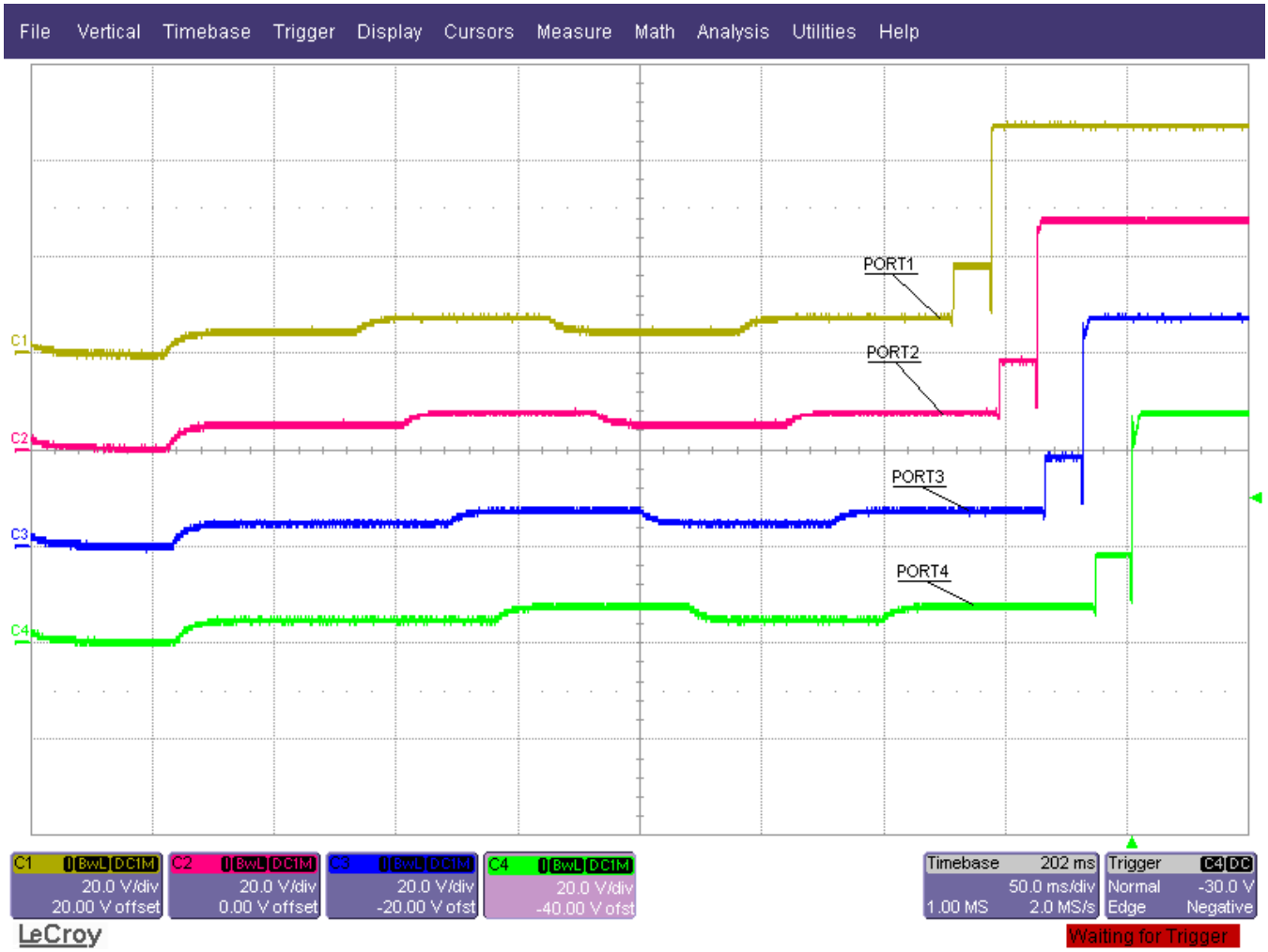


Figure 44. Port Sequencing after RESET Pin De-Assertion

7.4.5 Push-Button Power On Response

The port behavior of the TPS23861 to a commanded power on from the push-button register varies depending upon both the detect and class enable registers.

Table 8. Summarized Response(1)

OPERATING MODE	DETECT EN BIT	CLASS EN BIT	PORT BEHAVIOR
Off	x	x	Port does not power on
Manual	x	x	Port immediately powers on
Semi-Auto	0	0	Port does not power on
	1	0	Port powers on after completion of next good detect
	0	1	Port does not power on
	1	1	Port powers on after completion of next good detect and classification
Auto	x	x	Pushbutton power on ignored. Port follows Auto Mode rules

(1) Response to a push-button power on.

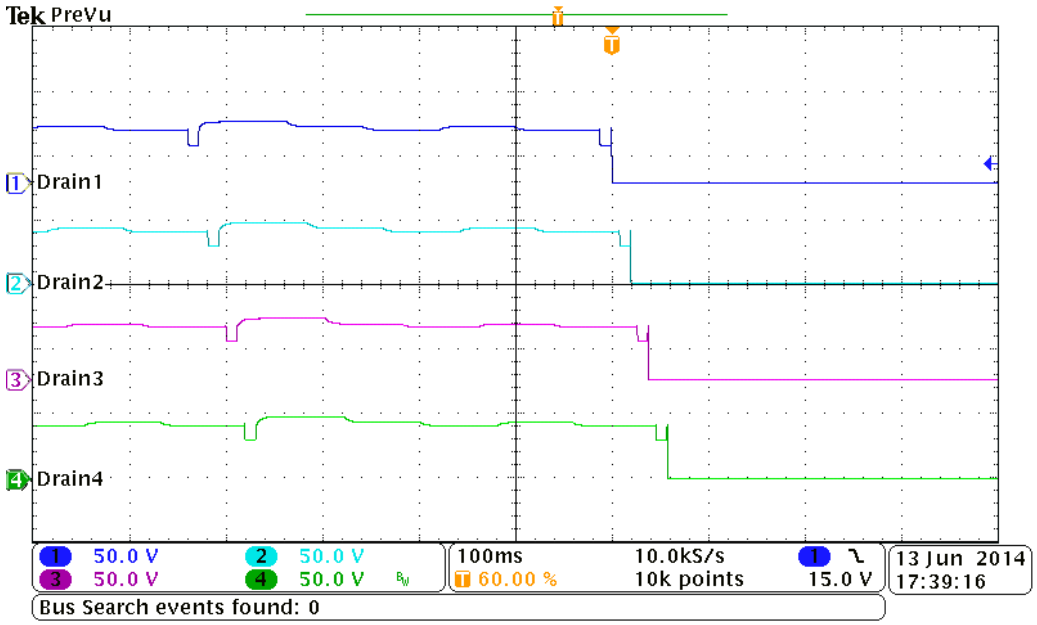


Figure 45. Semi-Auto Sequenced Turn On

7.4.6 TSTART Indicators of Detect and Class Failures

The start fault indicator reports additional problems in Semi-Auto and Auto Modes to the host. This notifies the host that the PSE encountered a problem and was unable to turn the port on. The interrupt pin activates when the TSTART mask is enabled and one of these fault conditions occur. The conditions are described in Table 9.

Table 9. Detect and Class Failure Indicators (1)

OPERATING MODE	FAULT CONDITION
Off	None
Manual	Overcurrent condition at the end of t_{START} time period
Semi-Auto	Overcurrent condition at the end of t_{START} time period
	Detect not valid
	Class unknown
	Class mismatch
	Class overcurrent
Auto	Overcurrent condition at the end of t_{START} time period
	Detect not valid
	Class unknown
	Class mismatch
	Class overcurrent

(1) Conditions that set start fault.

7.4.7 Device Power On Initialization

At device power on and after VDD and VPWR exceed V_{UVDDR} and V_{UVLOPW_R} respectively, TPS23861 initializes for t_{POR}. During this time TPS23861 will not respond to I^2C commands. Wait approximately 20 ms after t_{POR}, before sending I^2C commands.

7.5 Register Map – I²C-Addressable

Table 10. I²C-Addressable Register Set Summary (1)(2)

CMD CODE	REGISTER OR COMMAND NAME	I²C R/W	DATA BYTE	RST STATE	FIELD DESCRIPTION							
00	Interrupt	RO	1	1000,0000	SUPF	STRTF	IFAULT	CLASC	DETC	DISF	PGC	PEC
01	Interrupt Enable	R/W	1	1AA0,0A00	SUPEN	STRTEN	IFEN	CLCEN	DEEN	DISEN	PGSEN	PESEN
02	Power Event	RO	1	0000,0000	Power Good status change				Power Enable status change			
03		CoR	1		PGC4	PGC3	PGC2	PGC1	PEC4	PEC3	PEC2	PEC1
04	Detection Event	RO	1	0000,0000	Classification				Detection			
05		CoR	1		CLSC4	CLSC3	CLSC2	CLSC1	DETC4	DETC3	DETC2	DETC1
06	Fault Event	RO	1	0000,0000	Disconnect occurred				ICUT fault occurred			
07		CoR	1		DISF4	DISF3	DISF2	DISF1	ICUT4	ICUT3	ICUT2	ICUT1
08	Start/ILIM Event	RO	1	0000,0000	ILIM fault occurred				Start fault occurred			
09		CoR	1		ILIM4	ILIM3	ILIM2	ILIM1	STRT4	STRT3	STRT2	STRT1
0A	Supply Event	RO	1	0011,0000	TSD	-	VDUV	VPUV	-	-	-	-
0B		CoR	1									
0C	Port 1 Status	RO	1	0000,0000	CLASS P1				DETECT P1			
0D	Port 2 Status	RO	1	0000,0000	CLASS P2				DETECT P2			
0E	Port 3 Status	RO	1	0000,0000	CLASS P3				DETECT P3			
0F	Port 4 Status	RO	1	0000,0000	CLASS P4				DETECT P4			
10	Power Status	RO	1	0000,0000	PG4	PG3	PG2	PG1	PE4	PE3	PE2	PE1
11	I²C Slave Address	RO(3)	1	1010,0000	AUTO	SLA6	SLA5	SLA4	SLA3	SLA2	SLA1	SLA0
12	Operating Mode	R/W	1	AAAA,AAAA	Port 4 Mode		Port 3 Mode		Port 2 Mode		Port 1 Mode	
13	Disconnect Enable	R/W	1	0000,AAAA	-	-	-	-	DCDE4	DCDE3	DCDE2	DCDE1
14	Detect/Class ENABLE	R/W	1	AAAA,AAAA	CLE4	CLE3	CLE2	CLE1	DETE4	DETE3	DETE2	DETE1
15	Port PWR Priority	R/W	1	AAAA,0000	FSE4	FSE3	FSE2	FSE1	-	-	-	-
16	Timing Configuration	R/W	1	0000,0000	TLIM		TSTART		TICUT		TDIS	
17	General Mask	R/W	1	1000,0000	INTEN	-	-	MAINS	-	-	R	M250
18	Detect/Class Restart	WO	1	-	RCL4	RCL3	RCL2	RCL1	RDET4	RDET3	RDET2	RDET1
19	Power Enable	WO	1	-	POFF4	POFF3	POFF2	POFF1	PWON4	PWON3	PWON2	POWN1
1A	Reset	WO	1	-	CLRAIN	CLINP	-	RESAL	RESP4	RESP3	RESP2	RESP1
20	Legacy Detect Mode	R/W	1	0000,0000	LEGMOD4		LEGMOD3		LEGMOD2		LEGMOD1	
21	Two-Event Classification	R/W	1	0A0A,0A0A	TECLEN4		TECLEN3		TECLEN2		TECLEN1	
27	Interrupt Timer	R/W	1	0000,0000	R	R	R	R	TMR 3-0			
29	Disconnect Threshold	R/W	1	0000,0000	DCTH4		DCTH3		DCTH2		DCTH1	
2A	ICUT21 CONFIG	R/W	1	0000,0000	-	ICUT Port 2			-	ICUT Port 1		
2B	ICUT43 CONFIG	R/W	1	0000,0000	-	ICUT Port 4			-	ICUT Port 3		
2C	Temperature	RO		0000,0000	Temperature (bits 7 to 0)							

(1) Bits labeled "R" are reserved. Undesirable behavior may result if the value of these bits are changed from the reset value.
(2) Bits labeled "A" assume the state of the bit programmed into register 0x11 after POR.
(3) This register is Read/Write during slave address programming when preceded by the unlock code.

Register Map – I²C-Addressable (continued)

Table 10. I²C-Addressable Register Set Summary (1)(2) (continued)

CMD CODE	REGISTER OR COMMAND NAME	I²C R/W	DATA BYTE	RST STATE	FIELD DESCRIPTION
2E	Input Voltage	RO	2	0000,0000	Input voltage: LSByte
2F		RO		0000,0000	- - Input voltage: MSByte (bits 13 to 8)
30	Port 1 Current	RO	2	0000,0000	Port 1 current: LSByte
31		RO		0000,0000	- - Port 1 current: MSByte (bits 13 to 8)
32	Port 1 Voltage	RO	2	0000,0000	Port 1 voltage: LSByte
33		RO		0000,0000	- - Port 1 voltage: MSByte (bits 13 to 8)
34	Port 2 Current	RO	2	0000,0000	Port 2 current: LSByte
35		RO		0000,0000	- - Port 2 current: MSByte (bits 13 to 8)
36	Port 2 Voltage	RO	2	0000,0000	Port 2 voltage: LSByte
37		RO		0000,0000	- - Port 2 voltage: MSByte (bits 13 to 8)
38	Port 3 Current	RO	2	0000,0000	Port 3 current: LSByte
39		RO		0000,0000	- - Port 3 current: MSByte (bits 13 to 8)
3A	Port 3 Voltage	RO	2	0000,0000	Port 3 voltage: LSByte
3B		RO		0000,0000	- - Port 3 voltage: MSByte (bits 13 to 8)
3C	Port 4 Current	RO	2	0000,0000	Port 4 current: LSByte
3D		RO		0000,0000	- - Port 4 current: MSByte (bits 13 to 8)
3E	Port 4 Voltage	RO	2	0000,0000	Port 4 voltage: LSByte
3F		RO		0000,0000	- - Port 4 voltage: MSByte (bits 13 to 8)
40	PoE Plus	R/W	1	0000,----	POEP4 POEP3 POEP2 POEP1 - - - -
41	Firmware Revision	RO	1	RRRR,RRRR	Firmware revision
42	I²C Watchdog	R/W	1	0001,0110	- - - Watchdog disable WDS
43	Device ID	R/W	1	111,sr[4:0]	Device ID number Silicon revision number
45	Cool Down/Gate Drive	R/W	1	0000,0000	CLDN IGATE - - - - -
60	Port 1 Detect Resistance	RO	2	0000,0000	Port 1 resistance: LSByte
61		RO		0000,0000	RS1 Port 1 resistance: MSByte (bits 13 to 8)
62	Port 2 Detect Resistance	RO	2	0000,0000	Port 2 resistance: LSByte
63		RO		0000,0000	RS2 Port 2 resistance: MSByte (bits 13 to 8)
64	Port 3 Detect Resistance	RO	2	0000,0000	Port 3 resistance: LSByte
65		RO		0000,0000	RS3 Port 3 resistance: MSByte (bits 13 to 8)
66	Port 4 Detect Resistance	RO	2	0000,0000	Port 4 resistance: LSByte
67		RO		0000,0000	RS4 Port 4 resistance: MSByte (bits 13 to 8)
68	Port 1 Detect Voltage Difference	RO	2	0000,0000	Port 1 voltage difference (bits 7 to 0)
69		RO		0000,0000	VDS1 Port 1 voltage difference: MSByte (bits 11 to 8)
6A	Port 2 Detect Voltage Difference	RO	2	0000,0000	Port 2 voltage difference (bits 7 to 0)
6B		RO		0000,0000	VDS2 Port 2 voltage difference: MSByte (bits 11 to 8)
6C	Port 3 Detect Voltage Difference	RO	2	0000,0000	Port 3 voltage difference (bits 7 to 0)
6D		RO		0000,0000	VDS3 Port 3 voltage difference: MSByte (bits 11 to 8)
6E	Port 4 Detect Voltage Difference	RO	2	0000,0000	Port 4 voltage difference (bits 7 to 0)
6F		RO		0000,0000	VDS4 Port 4 voltage difference: MSByte (bits 11 to 8)

7.5.1 Interrupt Register

Command = 00h with 1 Data Byte, Read Only

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SUPF	STRTF	IFAULT	CLASC	DETC	DISF	PGC	PEC
RESET OR POR VALUE	1	0	0	0	0	0	0	0

Active high, each bit corresponds to a particular event that occurred.

Each bit can be individually reset by doing a read at the corresponding event register address, or by setting bit 7 of Reset Register.

Any active bit of the Interrupt register activates the $\overline{\text{INT}}$ output if its corresponding enable bit in the Interrupt Enable Register is set, as well as the INTEN bit in the General Mask Register.

Bit Descriptions

SUPF: Indicates that a supply event fault occurred.

SUPF = TSD || VDUV || VPUV

1 = At least one supply event fault occurred.

0 = No such event occurred.

STRTF: Indicates that a start fault occurred on at least one port.

STRTF = STRT1 || STRT2 || STRT3 || STRT4

1 = Start fault occurred for at least one port.

0 = No start fault occurred.

IFAULT: Indicates that an ICUT or ILIM fault occurred on at least one port.

IFAULT = ICUT1 || ICUT2 || ICUT3 || ICUT4 || ILIM1 || ILIM2 || ILIM3 || ILIM4

1 = ICUT or ILIM Fault occurred for at least one port.

0 = No ICUT or ILIM Fault occurred.

CLASC: Indicates that at least one classification cycle occurred on at least one port.

CLASC = CLSC1 || CLSC2 || CLSC3 || CLSC4

1 = At least one classification cycle occurred for at least one port.

0 = No classification cycle occurred.

DETC: Indicates that at least one detection cycle occurred on at least one port.

DETC = DETC1 || DETC2 || DETC3 || DETC4

1 = At least one detection cycle occurred for at least one port.

0 = No detection cycle occurred.

DISF: Indicates that a disconnect event occurred on at least one port.

DISF = DISF1 || DISF2 || DISF3 || DISF4

1 = Disconnect event occurred for at least one port.

0 = No disconnect event occurred.

PGC: Indicates that a power good status change occurred on at least one port.

PGC = PGC1 || PGC2 || PGC3 || PGC4

1 = Power good status change occurred on at least one port.

0 = No power good status change occurred.

PEC: Indicates that a power enable status change occurred on at least one port.

PEC = PEC1 || PEC2 || PEC3 || PEC4

1 = Power enable status change occurred on at least one port.

0 = No power enable status change occurred.

7.5.2 Interrupt Enable Register

Command = 01h with 1 Data Byte, Read/Write

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SUPEN	STRTEN	IFEN	CLCEN	DEEN	DISEN	PGSEN	PESEN
RESET or POR VALUE	1	A	A	0	0	A	0	0

Each bit corresponds to a particular event or fault as defined in the Interrupt Register.

Writing a 1 into a bit allows the corresponding event to generate an interrupt on the $\overline{INT}$ pin.

Writing a 0 into a bit masks the corresponding event/fault from activating the $\overline{INT}$ pin.

NOTE

The bits of the Interrupt Register always change state according to events or faults, regardless of the state of the Interrupt Enable Register. The INTEN bit of the General Mask 1 Register must also be set in order to allow an event to activate the $\overline{INT}$ output.

Bit Descriptions

SUPEN: Supply event fault enable bit.

1 = Supply event fault activates the $\overline{INT}$ output.

0 = Supply event fault has no impact on $\overline{INT}$ output.

STRTEN: Start fault enable bit.

1 = Start fault activates the $\overline{INT}$ output.

0 = Start fault has no impact on $\overline{INT}$ output.

IFEN: IFAULT enable bit.

1 = ICUT or ILIM Fault occurrence activates the $\overline{INT}$ output.

0 = ICUT or ILIM Fault occurrence has no impact on $\overline{INT}$ output.

CLCEN: Classification cycle interrupt enable bit.

1 = Classification cycle occurrence activates the $\overline{INT}$ output.

0 = Classification cycle occurrence has no impact on $\overline{INT}$ output.

DEEN: Detection cycle interrupt enable bit.

1 = Detection cycle occurrence activates the $\overline{INT}$ output.

0 = Detection cycle occurrence has no impact on $\overline{INT}$ output.

DISEN: Disconnect event interrupt enable bit.

1 = Disconnect event occurrence activates the $\overline{INT}$ output.

0 = Disconnect event occurrence has no impact on $\overline{INT}$ output.

PGSEN: Power good status change interrupt enable bit.

1 = Power good status change activates the $\overline{INT}$ output.

0 = Power good status change has no impact on $\overline{INT}$ output.

PESEN: Power enable status change interrupt enable bit.

1 = Power enable status change activates the $\overline{INT}$ output.

0 = Power enable status change has no impact on $\overline{INT}$ output.

7.5.3 Power Event Register

Command = 02h with 1 Data Byte, Read Only

Command = 03h with 1 Data Byte, Clear on Read

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	PGC4	PGC3	PGC2	PGC1	PEC4	PEC3	PEC2	PEC1
RESET or POR VALUE	0	0	0	0	0	0	0	0

Active high, each bit corresponds to a particular event that occurred.

Each bit PGCn, PECn represents an individual port.

A read at each location (02h or 03h) returns the same register data with the exception that the Clear-on-Read command clears all bits of the register.

If this register is causing the $\overline{INT}$ pin to be activated, this Clear-on-Read command releases the $\overline{INT}$ pin.

Any active bit will have an impact on the Interrupt Register as indicated in the Interrupt Register description.

Bit Descriptions

PGC4-PGC1: Indicates that a power good status change occurred.

1 = Power good status change occurred.

0 = No power good status change occurred.

PEC4-PEC1: Indicates that a power enable status change occurred.

1 = Power enable status change occurred.

0 = No power enable status change occurred.

7.5.4 Detection Event Register

Command = 04h with 1 Data Byte, Read Only

Command = 05h with 1 Data Byte, Clear on Read

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	CLSC4	CLSC3	CLSC2	CLSC1	DETC4	DETC3	DETC2	DETC1
RESET or POR VALUE	0	0	0	0	0	0	0	0

Active high, each bit corresponds to a particular event that occurred.

Each bit CLSCn, DETCn represents an individual port.

A read at each location (04h or 05h) returns the same register data with the exception that the Clear-on-Read command clears all bits of the register. These bits are cleared when port n is turned off.

If this register is causing the $\overline{INT}$ pin to be activated, this Clear-on-Read command releases the $\overline{INT}$ pin.

Any active bit will have an impact on the Interrupt Register as indicated in the Interrupt Register description.

Bit Descriptions

CLSC4-CLSC1: Indicates that at least one classification cycle occurred.

1 = At least one classification cycle occurred.

0 = No classification cycle occurred.

DETC4-DETC1: Indicates that at least one detection cycle occurred.

1 = At least one detection cycle occurred.

0 = No detection cycle occurred.

7.5.5 Fault Event Register

Command = 06h with 1 Data Byte, Read Only

Command = 07h with 1 Data Byte, Clear on Read

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	DISF4	DISF3	DISF2	DISF1	ICUT4	ICUT3	ICUT2	ICUT1
RESET or POR VALUE	0	0	0	0	0	0	0	0

Active high, each bit corresponds to a particular event that occurred.

Each bit DISFn, ICUTn represents an individual port.

A read at each location (06h or 07h) returns the same register data with the exception that the Clear-on-Read command clears all bits of the register. These bits are cleared by I^2C power-off command (POFFn) or port-reset command (RESPn).

If this register is causing the $\overline{INT}$ pin to be activated, this Clear-on-Read releases the $\overline{INT}$ pin.

Any active bit will have an impact on the Interrupt Register as indicated in the Interrupt Register description.

Bit Descriptions

DISF4-DISF1: Indicates that a disconnect event occurred.

1 = Disconnect event occurred.

0 = No disconnect event occurred.

ICUT4-ICUT1: Indicates that an ICUT Fault occurred.

1 = ICUT fault occurred.

0 = No ICUT fault occurred.

7.5.6 Start/ILIM Event Register

Command = 08h with 1 Data Byte, Read Only

Command = 09h with 1 Data Byte, Clear on Read

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	ILIM4	ILIM3	ILIM2	ILIM1	STRT4	STRT3	STRT2	STRT1
RESET or POR VALUE	0	0	0	0	0	0	0	0

Active high, each bit corresponds to a particular event that occurred.

Each bit ILIMn, STRTn represents an individual port.

A read at each location (08h or 09h) returns the same register data with the exception that the Clear-on-Read command clears all bits of the register. These bits are cleared by I^2C power-off command (POFFn) or port-reset command (RESPn).

If this register is causing the $\overline{INT}$ pin to be activated, this Clear-on-Read command releases the $\overline{INT}$ pin.

Any active bit has an impact on the Interrupt Register as indicated in the Interrupt Register description.

Bit Descriptions

STRT4-STRT1: Indicates that a start fault occurred at port turn on. This may be caused by:

1. Overcurrent (foldback) condition at the end of t_{START}.
2. Detect or classification fault following a pushbutton PWON command.
3. Detect fault or classification unknown, mismatch or overcurrent in Auto Mode.

1 = Inrush fault or class/detect error occurred.

0 = No inrush fault or class/detect error occurred.

ILIM4-ILIM1: Indicates that an ILIM fault occurred, which means the port has limited its output current to ILIM or the folded back ILIM for more than t_{LIM}.

1 = ILIM fault occurred.

0 = No ILIM fault occurred.

7.5.7 Supply Event Register

Command = 0Ah with 1 Data Byte, Read Only

Command = 0Bh with 1 Data Byte, Clear on Read

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	TSD	-	VDUV	VPUV	-	-	-	-
POR VALUE	0	0	1	1	0	0	0	0

Active high, each bit corresponds to a particular event that occurred.

A read at each location (0Ah or 0Bh) returns the same register data with the exception that the Clear-on-Read command clears all bits of the register.

If this register is causing the $\overline{INT}$ pin to be activated, this Clear-on-Read releases the $\overline{INT}$ pin.

Any active bit has an impact on Interrupt Register as indicated in the Interrupt Register description.

Bit Descriptions

TSD: Indicates that a thermal shutdown occurred. When there is thermal shutdown, all ports are powered off and are put in Off Mode. The TPS23861 internal circuitry continues to operate however, including the A/D converters. Note that at as soon as the internal temperature has decreased below the low threshold, the ports can be powered on regardless of the status of the TSD bit.

1 = Thermal shutdown occurred.

0 = No thermal shutdown occurred.

VDUV: Indicates that a VDD UVLO occurred. VDUV is set following a power-on reset or if the voltage at the VDD pin falls below V_{UVDD_F}

1 = VDD UVLO occurred.

0 = No VDD UVLO occurred.

VPUV: Indicates that a VPWR UVLO occurred. VPUV is set following a power-on reset or if the voltage at the VPWR pin falls below V_{PUV_F}.

1 = VPWR undervoltage occurred.

0 = No VPWR undervoltage occurred.

NOTE

If the $\overline{RESET}$ input is pulled low during normal operation, VPUV is set if VPWR is below its UVLO threshold. There is no impact on VDUV since VDD is maintained.

When VPWR drops below V_{PUV_F} but not as low as V_{UVLOPW_F} all ports are powered off as if a push-button off was executed. (Same as writing 1 to POFFn in Power Enable Register.) When VPWR undervoltage (below V_{UVLOPW_F}) occurs, all ports are powered off, and there is a power-on reset.

7.5.8 Port n Status Register

7.5.8.1 Port 1 Status Register

Command = 0Ch with 1 Data Byte, Read Only

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	CLASS P1				DETECT P1			
RESET or POR VALUE	0	0	0	0	0	0	0	0

7.5.8.2 Port 2 Status Register

Command = 0Dh with 1 Data Byte, Read Only

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	CLASS P2				DETECT P2			
RESET or POR VALUE	0	0	0	0	0	0	0	0

7.5.8.3 Port 3 Status Register

Command = 0Eh with 1 Data Byte, Read Only

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	CLASS P3				DETECT P3			
RESET or POR VALUE	0	0	0	0	0	0	0	0

7.5.8.4 Port 4 Status Register

Command = 0Fh with 1 Data Byte, Read Only

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	CLASS P4				DETECT P4			
RESET or POR VALUE	0	0	0	0	0	0	0	0

Represents the most recent classification and detection results for port n. These bits are cleared when port n is turned off.

NOTE

In order to disable detection for any port with unknown, short circuit, open circuit, or MOSFET fault detection status (0x0C-0x0F), clear the corresponding port DETEx bits in 0x14 instead of writing the port off command to 0x12, 0x19, or 0x1A.

Bit Descriptions

CLASS Pn[3:0]: CLASS Pn is a 4-bit field for each port. The value of CLASS Pn is the most recent classification result on port n. The selection is as following:

CLASS Pn	CLASSIFICATION STATUS
0000	Unknown
0001	Class 1
0010	Class 2
0011	Class 3
0100	Class 4
0101	Reserved – read as Class 0
0110	Class 0
0111	Overcurrent
1000	Class mismatch

A class mismatch can occur only during two-event classification. If the classification status for the first and second event are different, and the second classification status is not *Overcurrent*, the Classification Status is set to Class mismatch. If the status of the first classification event is “Overcurrent”, the classification status will be set to “Overcurrent” in the CLASS Pn, and there will be no second classification event in any case. In Auto Mode, port will not power on automatically, but still can be powered on through the Power Enable Register. The appropriate STRTn bit is set in the Start/ILIM Event Register following these sorts of faults during classification.

DETECT Pn[3:0]: DETECT Pn is a 4-bit field for each port. The value of DETECT Pn is the most recent detection result on port n.

NOTE

Bit states 1001 – 1100 apply to legacy detection only.

The selection is as following:

DETECT Pn	DETECT STATUS
0000	Unknown (POR value)
0001	Short circuit (<500 Ω)
0010	Reserved
0011	Resistance too low
0100	Resistance valid
0101	Resistance too high
0110	Open circuit
0111	Reserved
1000	MOSFET fault
1001	Legacy detect
1010	Capacitance measurement invalid: Detect measurement beyond clamp voltage
1011	Capacitance measurement invalid: Insufficient Δv measured
1100	Capacitance measurement is valid, but outside the range of a legacy device.

7.5.9 Power Status Register

Command = 10h with 1 Data Byte, Read Only

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	PG4	PG3	PG2	PG1	PE4	PE3	PE2	PE1
RESET or POR VALUE	0	0	0	0	0	0	0	0

Each bit represents the actual power status of a port.

Each bit PGn, PEn represents an individual port.

These bits are cleared when port n is turned off, including if the turn off is caused by a fault condition.

Bit Descriptions

PG4-PG1: Each bit, when at 1, indicates that the port is on and that the voltage at DRAINn has gone below VPGT while the port is powered on. These bits are latched high once the turn on is complete and can only be cleared when the port is turned off or following a reset or power-on reset.

1 = Power is good.

0 = Power is not good.

PE4-PE1: Each bit indicates the on/off state of the corresponding port.

1 = Port is on.

0 = Port is off.

7.5.10 I^2C Slave Address Register

Command = 11h with 1 Data Byte, Read Only

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	AUTO	SLA6	SLA5	SLA4	SLA3	SLA2	SLA1	SLA0
Initial EEPROM VALUE	1	0	1	0	0	0	0	0

Bit Descriptions

SLA6-SLA0: I^2C device address, stored in EEPROM . This address can be changed by following the I^2C slave address programming protocol. For more details, see the I^2C Slave Address and AUTO Bit Programming.

NOTE

The programmed device address should not be any of 0x00, 0x30, 0x0C.

AUTO: Defines whether the controller operates automatically in Auto Mode even in the absence of a host controller. Automatic operation is described in Independent Operation when the Bit is Set section. The state of this bit is monitored only immediately following a Power-on Reset or after the $\overline{\text{RESET}}$ input has been activated. The impact of that bit state on registers after reset is reflected in Table 10 and is referred to “A”.

DESCRIPTION	BINARY DEVICE ADDRESS						
	6	5	4	3	2	1	0
BROADCAST ACCESS	0	1	1	0	0	0	0
ALERT RESPONSE	0	0	0	1	1	0	0
SLAVE NUMBER	SLA6	SLA5	SLA4	A3 pin	SLA2	SLA1	SLA0

7.5.11 Operating Mode Register

Command = 12h with 1 Data Byte, R/W

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	Port 4 Mode		Port 3 Mode		Port 2 Mode		Port 1 Mode	
RESET or POR VALUE	AA		AA		AA		AA	

Each field configures the operating mode per port.

NOTE

An Operating Mode write command to 0x12 with a transition from Off Mode to Auto Mode or from Off Mode to Semi-Auto Mode requires an I^2C bus processing delay of 1.2 ms when followed by a Detect/Class Enable (0x14) write command. This delay applies from the end of the Operating Mode command (stop pulse) to the end of the Detect/Class Enable command (stop pulse).

Bit Descriptions

Port n Mode[1:0]: The selection is as following:

PORT n MODE [1:0]	OPERATING MODE
00	Off
01	Manual
10	Semi-Auto
11	Auto

In Off Mode, the port is off and there is neither detection nor classification. In Manual Mode, there is no automatic state change. In Semi-Auto Mode, detection and classification are automated but not the port power on, while in Auto Mode all three are automated. See Device Functional Modes for a detailed description of each of the four operating modes.

NOTE

For any port with power enable set (PEx=1 in 0x10), ensure that port power good status in 0x10 is also set (PGx=1) prior to changing the mode to Off in the Operating Mode register (0x12).

7.5.12 Disconnect Enable Register

Command = 13h with 1 Data Byte, R/W

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	-	-	-	-	DCDE4	DCDE3	DCDE2	DCDE1
RESET or POR VALUE	-	-	-	-	A	A	A	A

Enables the disconnect detection mechanism for each port.

Bit Descriptions

DCDE4-DCDE1: DC disconnect enable for each port. Disconnect consists of measuring the port current at SENn pin, starting the TDIS timer if this current is below a threshold and turning the port off if a time out occurs. Also, the corresponding disconnect bit (DISFn) in the Fault Event Register is set accordingly. The TDIS timer is reset each time the current goes higher than the disconnect threshold for 13% of T_{MPDO}. The counter does not decrement below zero. Look at the Timing Configuration Register for more details on how to set T_{MPDO} by writing to the TDIS field.

7.5.13 Detect/Class Enable Register

Command = 14h with 1 Data Byte, R/W

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	CLE4	CLE3	CLE2	CLE1	DETE4	DETE3	DETE2	DETE1
RESET or POR VALUE	A	A	A	A	A	A	A	A

Detection and classification enable for each port.

When in Manual mode, setting a bit means that only one cycle (detection or classification) is performed for the corresponding port. The bit is automatically cleared when the cycle has been completed.

NOTE

The same result can be obtained by writing to the Detect/Class Restart Register.

NOTE

Write commands to either 0x12, 0x18, 0x19, or 0x1A require an I^2C bus processing delay of 1.2 ms when followed by a Detect/Class Enable (0x14) write command. This delay applies from the end of the 0x12, 0x18, 0x19, or 0x1A command (stop pulse) to the end of the Detect/Class Enable command (stop pulse).

It is also cleared if a port turn off (Power Enable Register) is issued.

In Semi-Auto Mode, while the port is not powered up, detection and classification are performed continuously, as long as the CLEn and DETEn bits are kept set. First, detection is performed. If a *Resistance valid* status is returned, classification follows. After, the detect-class sequence repeats. If a valid status is not returned by the detection event, classification is skipped, and detection is repeated.

In Auto Mode, if the port is not powered up and the DETEn and CLEn bits are set, classification follows a valid detect, and power-on follows classification unless classification returns Unknown, Overcurrent or Class Mismatch Status.

During the cool-down cycle following a Start, ICUT or ILIM, any Detect/Class Enable command for that port are delayed until the end of the cool-down period.

NOTE

At the end of the cool-down period, one or more detection/class cycles are automatically restarted as described previously if the detect enable bit is set.

Bit Descriptions

CLE4-CLE1: Classification enable bits.

1 = Enabled.

0 = Disabled.

DETE4-DETE1: Detection enable bits.

1 = Enabled.

0 = Disabled.

7.5.14 Port Power Priority Register

Command = 15h with 1 Data Byte, R/W

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	FSE4	FSE3	FSE2	FSE1	R15[3]	R15[2]	R15[1]	R15[0]
RESET or POR VALUE	A	A	A	A	0	0	0	0

Bit Descriptions

FSE4-FSE1: Port power priority bits to support Fast Shutdown; one bit per port. It is used to specify which port or ports is/are shut down in response to an external assertion of the $\overline{\text{SHTDWN}}$ pin fast shutdown signal. The turn-off procedure is similar to a port reset using Reset command (Reset register). If one of these bits is set while the $\overline{\text{SHTDWN}}$ pin is low, that port is shut down as well.

1 = When the $\overline{\text{SHTDWN}}$ is forced to a low level, the corresponding port is powered off.

0 = $\overline{\text{SHTDWN}}$ signal has no impact on the port.

Reserved: Bits R15[3:0] are reserved for future use. Undesirable behavior may result if the value of these bits are changed from their reset value.

7.5.15 Timing Configuration Register

Command = 16h with 1 Data Byte, R/W

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	TLIM		TSTART		TICUT		TDIS	
RESET or POR VALUE	0	0	0	0	0	0	0	0

These bits define the timing configuration for all four ports.

NOTE

The PGn and PEn bits in the Power Status Register are cleared when there is a Start, ICUT or ILIM condition.

Bit Descriptions

TLIM[1:0]: ILIM fault timing, which is the foldback current limit time duration before port turn off. This timer is loaded with its maximum count corresponding to t_{LIM} after expiration of the t_{START} period; the timer counts down when the port is limiting its output current to ILIM. If the ILIM timer counts down to zero, the port is powered off. After the port is powered off the cool-down period commences. The cool-down period is selected by the CLDN field in the Cool Down/Gate Drive register. During the cool-down period the port will not engage in detection, classification, or powered-up operation. When the port is powered up and while the port current is below ILIM, the same counter increments at a rate $1/16^{th}$ of the count-down rate (independent of the setting in the CLDN field). The counter does not increment past the maximum count corresponding to the programmed TLIM value.

NOTE

At the end of the cool-down period, when in Semi-Auto or Auto Mode, a detection cycle is automatically restarted if the detect enable bit is set.

When a POEPn bit in the PoE Plus Register is cleared, the t_{LIM} used for the associated port is always the nominal value (~60 ms). If the POEPn bit is set, then t_{LIM} for associated port is programmable with the following selection:

TLIM[1:0]	NOMINAL t_{LIM} (ms) WHEN PoEPn BIT IS SET
00	60
01	30
10	15
11	10

TSTART[1:0]: This 2-bit field sets the length of the t_{START} period, which is the maximum allowed overcurrent time during inrush. If at the end of the t_{START} period the current is still limited to I_{INRUSH} , the port is powered off. This is followed by a cool-down period, set with the CLDN field in the Cool Down/Gate Drive Register, during which the port cannot be turned on if in Semi-Auto or Auto Mode.

NOTE

At the end of cool-down cycle, when in Semi-Auto or Auto Mode, a detection cycle is automatically restarted if the class and detect enable bits are set.

The selection is as following:

TSTART [1:0]	NOMINAL t_{START} (ms)
00	60
01	30
10	120
11	Reserved

TICUT[1:0]: ICUT fault timing, which is the overcurrent time duration before port turn off (t_{OVLD}).

This timer is loaded with its maximum count corresponding to t_{OVLD} after expiration of the t_{START} period; the timer counts down when the port current exceeds ICUT. If the ICUT timer counts down to zero, the port is powered off. After the port is powered off the cool-down period commences. The cool-down period is set with the CLDN field in the Cool Down/Gate Drive Register. During the cool-down period the port will not engage in detection, classification, or powered-up operation. When the port is powered up and while the port current is below ICUT, the same counter increments at a rate $1/16^{th}$ of the count-down rate (independent of the setting in the CLDN field). The counter does not increment past the maximum count corresponding to the programmed TICUT value.

NOTE

At the end of cool-down cycle, when in Semi-Auto or Auto Mode, a detection cycle is automatically restarted if the detect enable bit is set.

The selection is as following:

TICUT[1:0]	NOMINAL t_{OVLD} (ms)
00	60
01	30
10	120
11	240

TDIS[1:0]: Disconnect delay, which is the time to turn off a port once there is a disconnect condition.

After port power on and the completion of the t_{START} period the TDIS counter is started when the port current drops below the disconnect threshold established in the DCTHn fields, and the counter is reset each time the current goes continuously higher than the disconnect threshold for 13% of t_{MPDO}. The counter does not decrement below zero. The selection is as following:

TDIS[1:0]		NOMINAL t_{MPDO} (ms)
0	0	360
0	1	90
1	0	180
1	1	720

7.5.16 General Mask 1 Register

Command = 17h with 1 Data Byte, Read/Write

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	INTEN			MAINS	R17[3]	R17[2]	R17[1]	M250
RESET or POR VALUE	1	0	0	0	Reserved	Reserved	Reserved	0

Bit Descriptions

INTEN: $\overline{\text{INT}}$ pin enable bit. Writing a 1 permits any bit of the Interrupt Register to activate the $\overline{\text{INT}}$ output.

NOTE

Activating INTEN has no impact on the Event Registers.

1 = Any enabled bit of the Interrupt register can activate the $\overline{\text{INT}}$ output.

0 = $\overline{\text{INT}}$ output cannot be activated.

Reserved: Bits R17[3], R17[2] and R17[1] are reserved for future use. Undesirable behavior may result if the value of these bits are changed from the reset value.

MAINS: Detection Voltage Measurement Duration Bit. Set or clear this bit to correspond to the mains frequency local to where the TPS23861 is being used in a system. The A/D converter will perform 16 conversions during the detection cycle. The results of these 16 conversions are averaged resulting in a total acquisition time equal to one cycle of the mains frequency. This technique greatly reduces mains-induced interference in the detection cycle measurement.

1 = Convert port voltage during detection at a rate of 960 A/D conversions per second. This corresponds to 16 conversions during one period of 60-Hz mains frequency.

0 = Convert port voltage during detection at a rate of 800 A/D conversions per second. This corresponds to 16 conversions during one period of 50-Hz mains frequency.

M250: Current-sense-resistor-selection bit. Setting this bit directs the TPS23861 to use ICUT and classification look-up tables corresponding to a 250-mΩ current-sense resistor.

1 = Set this bit if a 250-mΩ current-sense resistor is used as a current-sense resistor.

0 = Clear this bit if a 255-mΩ current-sense resistor is used as a current-sense resistor.

7.5.17 Detect/Class Restart Register

Command = 18h with 1 Data Byte, Write Only

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	RCL4	RCL3	RCL2	RCL1	RDET4	RDET3	RDET2	RDET1

Push button register.

Each bit corresponds to a particular cycle (detect or class restart) per port.

Each cycle can be individually triggered by writing a “1” at that bit location, while writing a “0” does not change anything for that event.

In Manual Mode, a single cycle (detect or class restart) is initiated. In Semi-Auto and Auto Mode, the corresponding bit in the Detect/Class Enable register is set, and the TPS23861 operates as prescribed in Device Functional Modes section.

During the cool-down cycle following a Start, ICUT or ILIM, any Detect/Class Restart Command for that port is accepted, but the corresponding action is delayed until end of cool-down period.

NOTE

A Detect/Class Restart write command to 0x18 requires an I^2C bus processing delay of 1.2 ms when followed by a Detect/Class Enable (0x14) write command. This delay applies from the end of the Detect/Class Restart command (stop pulse) to the end of the Detect/Class Enable command (stop pulse).

Bit Descriptions

RCL4-RCL1: Restart classification bits.

RDET4-RDET1: Restart detection bits.

7.5.18 Power Enable Register

Command = 19h with 1 Data Byte, Write Only

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	POFF4	POFF3	POFF2	POFF1	PWON4	PWON3	PWON2	PWON1

Push button register. Setting a bit in this register directs the TPS23861 to turn a port on or off.

Used to force a port(s) power on or power off in any mode except Off Mode or during a port shutdown condition via the $\overline{\text{SHTDWN}}$ pin.

NOTE

A power off write command to 0x19 requires an I^2C bus processing delay of 1.2 ms when followed by a Detect/Class Enable (0x14) write command. This delay applies from the end of the power off command (stop pulse) to the end of the Detect/Class Enable command (stop pulse).

NOTE

In Semi-Auto or in Auto Mode, as long as the port is kept off, detection and classification are performed continuously if the corresponding class and detect enable bits are set.

The details of a power-on operation depends on the operating mode. See Device Functional Modes section for details.

Writing a “1” at POFFn location powers off the associated port.

NOTE

Writing a “1” at POFFn and PWONn of same port during the same write operation powers off the port.

During the cool-down cycle following a Start, ICUT or ILIM, when in Semi-Auto or Auto Mode, any port turn on using Power Enable Command is ignored. The port can be turned on at the end of the cool-down cycle. When in Manual Mode, the port powers on immediately in response to a power on command even when in cool-down.

Bit Descriptions

POFF4-POFF1: Port power off bits. When POFFn is written, the following takes place:

- The corresponding Port n Voltage Registers are cleared.
- The corresponding Port n Detect Resistance Register are cleared.
- The CLSCn and the DETCn bits in the Detection Event Register are cleared.
- The corresponding Port n Status Register are cleared.
- The CLEn and the DETEn bits in the Detect/Class Enable Register are cleared.
- The DISFn and ICUTn bits in the Fault Event Register are cleared.
- The ILIMn and the STRTN bits in the Start/ILIM Event Register are cleared.
- If the port was powered on when POFFn is set, the port is powered off, and the following occurs.
  - The PGCn and the PECn bits in the Power Event Register are set.
  - The PGn and PEn bits in the Power Status Register are cleared.

PWON4-PWON1: Port power on bits.

NOTE

For any port with power enable set (PEx=1 in 0x10), ensure that port power good status in 0x10 is also set (PGx=1) prior to writing a power off command to the Power Enable register (0x19).

7.5.19 Reset Register

Command = 1Ah with 1 Data Byte, Write Only

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	CLRAIN	CLINP		RESAL	RESP4	RESP3	RESP2	RESP1

Push button register.

Writing a “1” at a bit location triggers an event while a “0” has no impact.

NOTE

A reset port write command to 0x1A requires an I^2C bus processing delay of 1.2 ms when followed by a Detect/Class Enable (0x14) write command. This delay applies from the end of the reset port command (stop pulse) to the end of the Detect/Class Enable command (stop pulse).

Bit Descriptions

CLRAIN: Clear all interrupts bit. Writing a “1” to CLRAIN clears all event registers and all bits in the Interrupt Register. It also releases the $\overline{INT}$ pin.

CLINP: When a “1” is written to this register, the TPS23861 releases the $\overline{INT}$ pin without any impact on either the event registers nor on the Interrupt Register.

RESAL: Reset register bits when a “1” is written to this location. Writing a “1” to this location results in a state equivalent to a power-up reset.

NOTE

For any port with power enable set (PEx=1 in 0x10), ensure that port power good status in 0x10 is also set (PGx=1) prior to writing a reset port command to the Reset register (0x1A).

NOTE

The VDUV and VPUV bits (Supply Event Register) follow the state of VDD and VPWR supply rails.

RESP4-RESP1: Reset port bits. Used to force an immediate port(s) turn off in any mode, by writing a “1” at the corresponding RESPn bit location(s). When port n is reset, the following takes place.

- The corresponding Port n Voltage Register are cleared.
- The CLCSn and the DETCn bits in the Detection Event Register are cleared.
- The corresponding Port n Status Register are cleared.
- The CLEn and the DETEn bits in the Detect/Class Enable Register are cleared.
- The DISFn and ICUTn bits in the Fault Event Register are cleared.
- The ILIMn and STRTn bits in the Start/ILIM Event Register are cleared.
- If in cool-down, the lockout functionality of the cool-down timer is cancelled.
- If the port was powered on when RESPn is set, the port is shut off, and the following occurs.
  - The PGCn and the PECn bits in the Power Event Register are set.
  - The PGn and PEn bits in the Power Status Register are cleared.

7.5.20 Legacy Detect Mode Register

Command = 20h with 1 Data Byte, Read/Write

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	LEGMOD4		LEGMOD3		LEGMOD2		LEGMOD1	
RESET or POR VALUE	00		00		00		00	

Legacy-detect operation is described in Legacy Device Detection. The TPS23861 can perform a legacy-detect operation only or a standard detection followed by a legacy-detect operation when directed by the RDETn push-button command in the Detect/Class Restart Register, or in Semi-Auto or Auto Mode when the DETEn bit in the Detect/Class Enable Register is set. Note that in Semi-Auto or in Auto Mode, the port will not automatically power up if a legacy device is detected. In these cases, the port must be powered on by the host.

Bit Descriptions

LEGMODn[1:0]: Legacy-detection-mode field. This field defines the Legacy-Detect Mode of Port n as follows.

LEGMODn[1:0]	LEGACY DETECT MODE
00	Legacy detect disabled; if DETEn bit in Detect/Class Enable Register is set, a standard (resistance only) detection sequence will be performed.
01	Legacy detect sequence only; if DETEn bit in Detect/Class Enable Register is set, a legacy detect sequence will be performed
10	Standard + legacy detect sequence; if DETEn bit in Detect/Class Enable Register is set, a standard detection followed by legacy detect sequence will be performed
11	Reserved

7.5.21 Two-Event Classification Register

Command = 21h with 1 Data Byte, Read/Write

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	TECLEN4		TECLEN3		TECLEN2		TECLEN1	
RESET or POR VALUE	0A		0A		0A		0A	

The Two-Event Classification Register controls whether a second physical-layer classification event occurs after a class 4 PD is classified under the following circumstances:

- In Manual Mode, when CLEn is set or a pushbutton RCLn bit is written.
- In Semi-Auto Mode, when a PWONn pushbutton command is written.
- In Auto Mode.

Bit Descriptions

TECLENn[1:0]: The TECLENn field sets the conditions for PSE-initiated two-event physical layer classification as follows. The details of these conditions depend on the operating mode as outlined in the preceding paragraph and the Device Functional Modes section.

Table 11. TECLENn Field Encoding

TECLENn[1:0]	CONDITIONS FOR TWO-EVENT PHYSICAL-LAYER CLASSIFICATION
00	Two-event physical-layer classification is disabled
01	A second classification event is initiated if a class 4 classification event occurs
10	Reserved
11	A second classification event is initiated if a class 4 classification event occurs

7.5.22 Interrupt Timer Register

Command = 27h with 1 Data Byte, Read/Write

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	R27[7]	R27[6]	R27[5]	R27[4]	TMR[3]	TMR[2]	TMR[1]	TMR[0]
RESET OR POR VALUE	0	0	0	0	0	0	0	0

Bit Descriptions

TMR[3:0]: Non-critical interrupts may be deferred using an internal timer. Once loaded with a non-zero value, the internal timer counts continuously with period calculated as follows:

$$t = N \times t_{STEP}$$

where

- t = Timer period, ms
- N = 4-bit value in TMR[3:0] field
- t_{STEP} = 10 ms (1)

Non-critical interrupts generated within the TPS23861 will be passed to the interrupt-handling hardware whenever the timer counts down to 0. (The timer then reloads and continues to count.)

NOTE

'interrupt-handling hardware' includes all interrupt-enabling functionality as well.

Critical and non-critical interrupts are defined in Table 6. When the TMR[3:0] field is read, the contents will be the contents last written by firmware.

When TMR[3:0] = 0 all interrupts will be handled as they are generated. In other words, this function is disabled when TMR[3:0] = 0000.

Reserved: Bits R27[7:4] are reserved for future use. Undesirable behavior may result if the value of these bits are changed from the reset value.

7.5.23 Disconnect Threshold Register

Command = 29h with 1 Data Byte, Read/Write

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	DCTH4		DCTH3		DCTH2		DCTH1	
RESET or POR VALUE	00		00		00		00	

Disconnect current thresholds may be programmed individually for each port.

7.5.23.1 Bits Description

DCTHn[1:0]: A 2-bit field used to set the current threshold for disconnect. If the port is powered on and the current goes below the disconnect threshold set by DCTHn, the TDIS counter is started. If the TDIS timer times out the port is powered down.

DCTHn FIELD	DISCONNECT THRESHOLD, mA
00	7.5
01	15
10	30
11	50

7.5.24 ICUTnm CONFIG Register

7.5.24.1 ICUT21 CONFIG Register

Command = 2Ah with 1 Data Byte, Read/Write

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME		ICUT Port 2				ICUT Port 1		
RESET or POR VALUE	0	0	0	0	0	0	0	0

7.5.24.2 ICUT43 CONFIG Register

Command = 2Bh with 1 Data Byte, Read/Write

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME		ICUT Port 4				ICUT Port 3		
RESET or POR VALUE	0	0	0	0	0	0	0	0

7.5.24.3 Bits Description

ICUT Port n[2:0]: is a 3-bit field used to set the ICUT current threshold. If the current threshold set by ICUT Port n is exceeded, the TICUT timer begins to count. When the terminal count (0) is reached, an ICUT fault is declared, and the port is shut down.

NOTE

The current values in the following table are nominal values.

ICUT PORT n FIELD	I_{CUT} (mA)	PoEPn (1)
000	374	0
001	110	0
010	204	0
011	374	0
100	754	1
101	592	1
110	645	1
111	920	1

(1) PoEPn bit should be set according to ICUT value for host to ensure the ICUT and ILIM relationship.

7.5.25 Temperature Register

Command = 2Ch with 1 Data Byte, Read Only

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	Temp[7:0]							
RESET or POR VALUE	0	0	0	0	0	0	0	0

Die temperature register.

Bit Descriptions

Temp[7:0]: 8-bit data conversion result of temperature. The equation defining the temperature measured is:

$$T = -20 + N \times T_{STEP} \quad (2)$$

where

- T = temperature, °C
- TSTEP = LSB value
- N = 8-bit value in Temp[7:0]

MODE	FULL SCALE VALUE	LSB VALUE
Any	150°C (typical)	0.7°C

NOTE

Temperature sensor performance is only typical, not production tested and not ensured.

7.5.26 Input Voltage Register

Command = 2Eh with 2 Data Byte (LSByte first, MSByte second), Read Only

LSB: 2Eh

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	Input Voltage[7:0]							
RESET or POR VALUE	0	0	0	0	0	0	0	0

MSB: 2Fh

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME			Input Voltage[13:8]					
RESET or POR VALUE	0	0	0	0	0	0	0	0

Bit Descriptions

Data conversion result. The I^2C data transmission is a 2-byte transfer.

Input Voltage[13:0]: 14-bit Data conversion result of input voltage. The update rate is approximately 1 per second.

The equation defining the voltage measured is:

$$V = N \times V_{STEP} \quad (3)$$

where

- V = input voltage, V
- N = 14 bit value in input voltage register
- V_{STEP} = LSB value

MODE	FULL SCALE VALUE	LSB VALUE
Any	60 V	3.662 mV

NOTE

The measurement is made between VPWR and AGND.

7.5.27 Port n Current Register

7.5.27.1 Port 1 Current Register

Command = 30h with 2 Data Byte (LSByte first, MSByte second), Read Only

LSB: 30h

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	Port 1 Current[7:0]							
RESET or POR VALUE	0	0	0	0	0	0	0	0

MSB: 31h

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME			Port 1 Current[13:8]					
RESET or POR VALUE	0	0	0	0	0	0	0	0

7.5.27.2 Port 2 Current Register

Command = 34h with 2 Data Byte (LSByte first, MSByte second), Read Only

LSB: 34h

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	Port 2 Current[7:0]							
RESET or POR VALUE	0	0	0	0	0	0	0	0

MSB: 35h

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	-	-	Port 2 Current[13:8]					
RESET or POR VALUE	0	0	0	0	0	0	0	0

7.5.27.3 Port 3 Current Register

Command = 38h with 2 Data Byte (LSByte first, MSByte second), Read Only

LSB: 38h

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	Port 3 Current[7:0]							
RESET or POR VALUE	0	0	0	0	0	0	0	0

MSB: 39h

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME			Port 3 Current[13:8]					
RESET or POR VALUE	0	0	0	0	0	0	0	0

7.5.27.4 Port 4 Current Register

Command = 3Ch with 2 Data Byte (LSByte first, MSByte second), Read Only

LSB: 3Ch

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	Port 4 Current[7:0]							
RESET or POR VALUE	0	0	0	0	0	0	0	0

MSB: 3Dh

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME			Port 4 Current[13:8]					
RESET or POR VALUE	0	0	0	0	0	0	0	0

Port current is monitored continuously when:

- The port is powered on.
- The port is in Off Mode. Data conversion result.

The I^2C data transmission is a 2-byte transfer.

NOTE

The conversion is done using a TI-proprietary multi-slope integrating converter.

Bit Descriptions

Port n Current[13:0]: 14-bit data conversion result of current for Port n. The result depends on whether the current-sense resistor is 250 mΩ or 255 mΩ.

The equation defining the current measured is:

$$I = N \times I_{STEP} \quad (4)$$

where

- I = Port n Current, A
- N = 14-bit value in Port n Current Register
- I_{STEP} = LSB value

R_S = 255 mΩ		R_{SENSE} = 250 mΩ	
FULL SCALE	LSB VALUE	FULL SCALE	LSB VALUE
1 A	61.039 µA	1.02 A	62.260 µA

7.5.28 Port n Voltage Register

7.5.28.1 Port 1 Voltage Register

Command = 32h with 2 Data Byte (LSByte first, MSByte second), Read Only

LSB: 32h

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	Port 1 Voltage[7:0]							
RESET or POR VALUE	0	0	0	0	0	0	0	0

MSB: 33h

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME			Port 1 Voltage[13:8]					
RESET or POR VALUE	0	0	0	0	0	0	0	0

7.5.28.2 Port 2 Voltage Register

Command = 36h with 2 Data Byte (LSByte first, MSByte second), Read Only

LSB: 36h

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	Port 2 Voltage[7:0]							
RESET or POR VALUE	0	0	0	0	0	0	0	0

MSB: 37h

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME			Port 2 Voltage[13:8]					
RESET or POR VALUE	0	0	0	0	0	0	0	0

7.5.28.3 Port 3 Voltage Register

Command = 3Ah with 2 Data Byte (LSByte first, MSByte second), Read Only

LSB: 3Ah

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	Port 3 Voltage[7:0]							
RESET or POR VALUE	0	0	0	0	0	0	0	0

MSB: 3Bh

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME			Port 3 Voltage[13:8]					
RESET or POR VALUE	0	0	0	0	0	0	0	0

7.5.28.4 Port 4 Voltage Register

Command = 3Eh with 2 Data Byte (LSByte first, MSByte second), Read Only

LSB: 3Eh

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	Port 4 Voltage[7:0]							
RESET or POR VALUE	0	0	0	0	0	0	0	0

MSB: 3Fh

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME			Port 4 Voltage[13:8]					
RESET or POR VALUE	0	0	0	0	0	0	0	0

Port voltage is monitored continuously when

- The port is powered on.
- The port is in Off Mode.

Data conversion result. The I^2C data transmission is a 2-byte transfer.

Bit Descriptions

Port n Voltage[13:0]: 14-bit Data conversion result of voltage for port n. The equation defining the voltage measured is:

$$V = N \times V_{STEP}$$

where

- V = Port n Voltage, V
- N = 14-bit value in Port n Voltage Register
- V_{STEP} = LSB Value (5)

FULL SCALE VALUE	LSB VALUE
60 V	3.662 mV

NOTE

The port voltage measurement is made between VPWR and DRAINn.

7.5.29 PoE Plus Register

Command = 40h with 1 Data Byte, R/W

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	PoEP4	PoEP3	PoEP2	PoEP1				
RESET or POR VALUE	0	0	0	0				

The POEPn bit can be set or cleared by the host processor over the I^2C interface. Additionally, the bit is set when in Auto Mode before the port is powered on following the recognition of a valid Class 4 PD. Likewise, the POEPn bit is cleared before the port is powered on when in Auto Mode and a Class 0, 1, 2 or 3 PD is recognized.

One POEPn bit supports each port. When the POEPn bit for a port is set:

- 2 x I_{LIM} foldback curve is applied to a port when the port is powered on. See Figure 58.
- The short-circuit protection threshold (I_{LIM}) for the FET is increased by a factor of 2.5 with respect to the POEPn-bit-cleared value.
- The t_{LIM} value is selectable via the TLIM timer field in the Timing Configuration Register.

Likewise, when the POEPn bit for a port is cleared:

- 1 x I_{LIM} foldback curve is applied to a port when the port is powered on. See Figure 58.
- The short-circuit protection threshold (I_{LIM}) for the FET is reduced to a value of 40% of the POEPn-bit-set value.
- The t_{LIM} value is set to 60 ms.

The inrush-foldback behavior is not affected by the setting of the POEPn bit. See Figure 57.

Bit Descriptions

PoEPn: PoE+ bits. Setting this bit causes the 2 x I_{LIM} foldback curve to be applied to Port n.

1 = Use 2 x I_{LIM} foldback curve on Port n.

0 = Use 1 x I_{LIM} foldback curve on Port n.

NOTE

PoEPn bit should be set according to ICUT value for host to ensure the ICUT and ILIM relationship. See Table 15

7.5.30 Firmware Revision Register

Command = 41h with 1 Data Byte, Read Only

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME						FRV		
RESET or POR VALUE	R	R	R	R	R	RRR		

Bit Descriptions

FRV[2:0]: Firmware revision number.

7.5.31 I²C Watchdog Register

Command = 42h with 1 Data Byte, R/W

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME				IWD[3:0]				WDS
RESET or POR VALUE				1	0	1	1	0

The I²C watchdog timer monitors the I²C clock line in order to prevent hung software situations that could leave ports in a hazardous state. The timer can be reset by either edge on SCL input. If the watchdog timer times out, the WDS bit is set. Depending on the value of IWD, all ports may be powered down. The nominal watchdog time-out period is 2 seconds.

When the ports are powered down due to a watchdog event, the corresponding bits are cleared in the Detection Event Register (CLSCn, DETn), Fault Event register (DISFn, ICUTn), Start/ILIM Event Register (STRTn), Port n Status Registers (Class Pn, Detect Pn) and Detect/Class Enable Register (CLEn, DETEn).

The corresponding PEn and PGn bits of the Power Status Register are also updated accordingly.

Bit Descriptions

IWD3 - IWD0: I²C Watchdog disable. When equal to 1011, the watchdog is masked. Otherwise, it is umasked and the watchdog is operational.

WDS: I²C Watchdog timer status, valid even if the watchdog is masked. When set, it means that the watchdog timer has expired without any activity on I²C clock line. Writing 0 at WDS location clears it.

NOTE

when the watchdog timer expires and if the watchdog is unmasked, all ports are also turned off.

When the ports are turned OFF due to I²C watchdog, the corresponding bits in Detection Event Register (CLSCn, DETCn), Fault Event Register (DISFn, ICUTn), Start Event Register (STRTn), Port n Status register (Class Pn, Detect Pn), Detect/Class Enable Register (CLEn, DETEn) and Power-On Fault Register (PFn) are also cleared. The corresponding PGCn and PECn bits of Power Event register is set if there is a change. The corresponding PEn and PGn bits of Power Status Register are updated accordingly

7.5.32 Device ID Register

Command = 43h with 1 Data Byte, R/W

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	DID			SR				
RESET or POR VALUE	1	1	1	SR[4:0]				

Bit Descriptions

DID: Device ID number (111).

SR: Silicon Revision number.

7.5.33 Cool Down/Gate Drive Register

Command = 45h with 1 Data Byte, R/W

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	CLDN		IGATE					
RESET or POR VALUE	0	0	0	0	0	0	0	0

These bits are applicable to all four ports.

Bit Descriptions

CLDN: Fault Cool-Down Timer Programming Field. Following a Start, ICUT or ILIM, a port shuts down, and the cool-down timer counts down. Until the timer counts down to 0, the port will not be allowed to be powered on if the port is in Semi-Auto or Auto Mode. If in Manual Mode, the port can be powered on immediately with a push-button command by writing to PWONn in the Power Enable Register. The cool-down timer is cancelled by power-on reset, device reset or port reset (see Reset Register).

The field programming is:

CLDN[1:0]	NOMINAL COOL-DOWN TIMER PERIOD
0X	1 s
10	2 s
11	4 s

IGATE: GATE Pull-Up Current Bit. IGATE sets the gate pull-up current.

IGATE	NOMINAL GATE PULLUP CURRENT (µA)
0	50
1	25

7.5.34 Port n Detect Resistance Register

7.5.34.1 Port 1 Detect Resistance Register

Command = 60h with 2 Data Byte (LSByte first, MSByte second), Read Only

LSB: 60h

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	Port 1 Resistance[7:0]							
RESET or POR VALUE	0	0	0	0	0	0	0	0

MSB: 61h

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	RS1[1:0]		Port 1 Resistance[13:8]					
RESET or POR VALUE	0	0	0	0	0	0	0	0

7.5.34.1.1 Port 2 Detect Resistance Register

Command = 62h with 2 Data Byte (LSByte first, MSByte second), Read Only

LSB: 62h

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	Port 2 Resistance[7:0]							
RESET or POR VALUE	0	0	0	0	0	0	0	0

MSB: 63h

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	RS2[1:0]		Port 2 Resistance[13:8]					
RESET or POR VALUE	0	0	0	0	0	0	0	0

7.5.34.1.2 Port 3 Detect Resistance Register

Command = 64h with 2 Data Byte (LSByte first, MSByte second), Read Only

LSB: 64h

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	Port 3 Resistance[7:0]							
RESET or POR VALUE	0	0	0	0	0	0	0	0

MSB: 65h

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	RS3[1:0]		Port 3 Resistance[13:8]					
RESET or POR VALUE	0	0	0	0	0	0	0	0

7.5.34.1.3 Port 4 Detect Resistance Register

Command = 66h with 2 Data Byte (LSByte first, MSByte second), Read Only

LSB: 66h

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	Port 4 Resistance[7:0]							
RESET or POR VALUE	0	0	0	0	0	0	0	0

MSB: 67h

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	RS4[1:0]		Port 4 Resistance[13:8]					
RESET or POR VALUE	0	0	0	0	0	0	0	0

Bit Descriptions

Most recent 2 point detection resistance measurement. The resistance value shown is usable only if RSn[1:0] are at 00 or 01. The I^2C data transmission is a 2 byte transfer.

Port n Resistance[13:0]: 14-bit data conversion result of detection resistance for port n. The equation defining the resistance measured is:

$$R = N \times R_{STEP} \quad (6)$$

where

- R = Detection resistance, Ω
- N = 14-bit value in Port n Resistance Register
- R_{STEP} = LSB value

USEABLE RESISTANCE RANGE	LSB VALUE
500 Ω to 55 kΩ	11.0966 Ω

RSn[1:0]: Most recent detection result status on port n. If the state is 00, the 14-bit resistance value is calculated with a bit weight of 11.0966 Ω/bit. If the state is 01, two additional detection fingers have been performed at higher detection currents (270 µA and 540 µA) in order to better measure the lower port impedance. The 14-bit resistance value is calculated with a bit weight of 4.625 Ω/bit in this case. The detection result is maintained in the register in any operating mode following the detection.

R_{Sn1}	R_{Sn0}	DETECT STATUS	R_{STEP} BIT WEIGHT
0	0	Other	11.0966 Ω/bit
0	1	Low (< 2 kΩ)	Additional detect 4.625 Ω/bit
1	0	Open circuit	N/A
1	1	MOSFET short fault	N/A

7.5.35 Port n Detect Voltage Difference Register

7.5.35.1 Port 1 Detect Voltage Difference Register

Command = 68h with 2 Data Byte (LSByte first, MSByte second), Read Only

LSB: 68h

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	Port 1 Voltage Difference [7:0]							
RESET or POR VALUE	0	0	0	0	0	0	0	0

MSB: 69h

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	VDS1[3:0]				Port 1 Voltage Difference [11:8]			
RESET or POR VALUE	0	0	0	0	0	0	0	0

7.5.35.2 Port 2 Detect Voltage Difference Register

Command = 6Ah with 2 Data Byte (LSByte first, MSByte second), Read Only

LSB: 6Ah

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	Port 2 Voltage Difference [7:0]							
RESET or POR VALUE	0	0	0	0	0	0	0	0

MSB: 6Bh

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	VDS2[3:0]				Port 2 Voltage Difference [11:8]			
RESET or POR VALUE	0	0	0	0	0	0	0	0

7.5.35.3 Port 3 Detect Voltage Difference Register

Command = 6Ch with 2 Data Byte (LSByte first, MSByte second), Read Only

LSB: 6Ch

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	Port 3 Voltage Difference [7:0]							
RESET or POR VALUE	0	0	0	0	0	0	0	0

MSB: 6Dh

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	VDS3[3:0]				Port 3 Voltage Difference [11:8]			
RESET or POR VALUE	0	0	0	0	0	0	0	0

7.5.35.4 Port 4 Detect Voltage Difference Register

Command = 6Eh with 2 Data Byte (LSByte first, MSByte second), Read

LSB: 6Eh

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	Port 4 Voltage Difference [7:0]							
RESET or POR VALUE	0	0	0	0	0	0	0	0

MSB: 6Fh

BITS	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	VDS4[3:0]				Port 4 Voltage Difference [11:8]			
RESET or POR VALUE	0	0	0	0	0	0	0	0

This register is used to determine the presence of a legacy PD by measuring the PD input capacitance on the PI. A charge is injected into the PI, and the resulting Δv is reported. The Δv value shown is useable only if VDSn[3:0] = 0001.

The I^2C data transmission is a 2-byte transfer.

Bit Descriptions

Port n Voltage Difference[11:0]: 12-bit data conversion result of the difference in voltage on the port as a result of a fixed charge injected into the port. The equation defining the resistance measured is:

$$C \cong \frac{k}{N \times V_{STEP}} \quad (7)$$

where

- C = Port capacitance, F
- k = 81 x 10-6 coulomb
- N = 12-bit value in Port n Detect Voltage Difference Register
- V_{STEP} = LSB Value

NOTE

The expression for port capacitance ignores the effect of any conductance in parallel with the capacitance being measured. The effect of parallel conductance is to give a higher value than the actual value of any capacitance present.

USEABLE CAPACITANCE RANGE	VOLTAGE DIFFERENCE LSB VALUE
10 to 100 µF	4.884 mV

VDSn[3:0]: Most recent detect voltage difference result status on Port n. If “0001” state, the 12-bit Δv value is useable.

This measurement is made on a port if legacy detect is enabled using the Legacy Detect Mode Register.

VDSn is set to the Power-On Reset State (0000b) when legacy detection is enabled until a Δv measurement is made.

The detection result is maintained in the register in any operating mode following the measurement.

The selection is as following:

VDSn[3:0]	VOLTAGE-DIFFERENCE MEASUREMENT STATUS
0000	Power-on reset
0001	Valid measurement
0010	Unable to discharge PD input capacitance to 2.4 V before timeout
0011	Unable to achieve 0.4V to take first measurement before timeout
0100	First measurement exceeds VDet-clamp (min)
0101	Second measurement exceeds VDet-clamp (min)
0110	ΔV < 0.5 V (insufficient signal)

7.5.36 Reserved Registers

- Register 0x1B
- Register 0x1D
- Register 0x1E
- Register 0x1F
- Register 0x22
- Register 0x23
- Register 0x24
- Register 0x25
- Register 0x59

Reserved: These registers are reserved for manufacturing or future use. Undesirable behavior may result if these registers are written to.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Introduction to PoE

Power-over-Ethernet (PoE) is a means of distributing power to Ethernet devices over the Ethernet cable using either data or spare pairs. PoE eliminates the need for power supplies at the Ethernet device. Common applications of PoE are security cameras, IP Phones and PDA chargers. The host or mid-span equipment that supplies power is the Power Source Equipment (PSE). The load at the Ethernet connector is the Powered device (PD). PoE protocol between PSE and PD controlling power to the load is specified by IEEE Std 802.3at-2009. Transformers are used at Ethernet host ports, mid-spans and hubs, to interface data to the cable. A DC voltage can be applied to the center tap of the transformer with no effect on the data signals. As in any power transmission line, a relatively high 48 V is used to keep current low, minimize the effect of IR drops in the line and preserve power to the load. Standard POE delivers approximately 13 W to a type 1 PD, and 25.5 W to a type 2 PD. Figure 46 shows the overview schematic of a POE port.

8.2 Application Information

The TPS23861 is a four port, IEEE 802.3at PoE PSE controller and can be used in very simple, low port count, automatic or high port count micro-controller managed applications.

Subsequent sections describe detailed design procedures for applications with different requirements including host control.

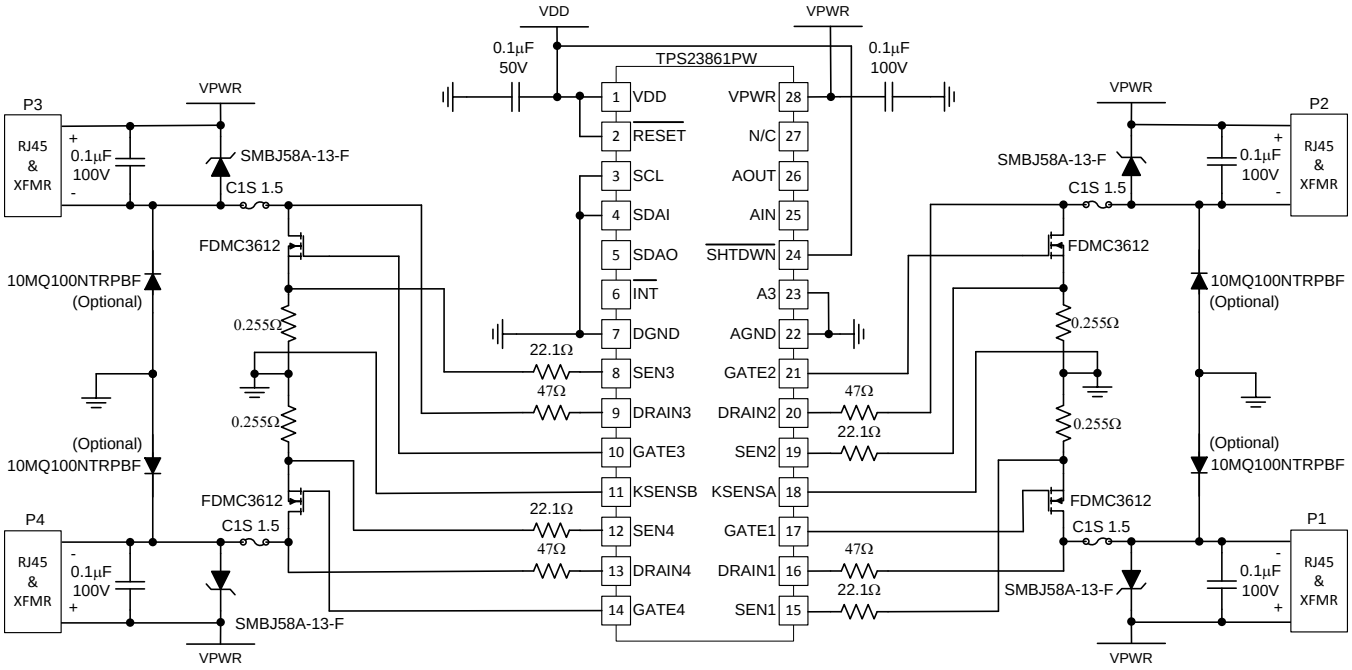


Figure 46. Automatic 4-Port Operation Schematic

Application Information (continued)

The schematic of Figure 46 depicts automatic mode operation of the TPS23861, providing turnkey functionality ready to power PoE loads. No connection to the I^2C bus or any type of host control is required. In Figure 46 the TPS23861 automatically:

1. Performs load detection.
2. Performs classification including type-2 (two-finger) of up to Class 4 loads.
3. Enables power with protective foldback current limiting, and ICUT value based on load class.
4. Shuts down in the event of fault loads and shorts.
5. Performs *Maintain Power Signature* function to ensure removal of power if load is disconnected.
6. Undervoltage lock out occurs if VPWR falls below V_{PUV_F} (typical 26.5 V).

Following a power-off command, disconnect or shutdown due to a start, ICUT or ILIM fault, the port powers down. Following port power off due to a power off command or disconnect, the TPS23861 continues automatic operation starting with a detection cycle. If the shutdown is due to a start, ICUT or ILIM fault, the TPS23861 enters into a cool-down period. After the end of the cool-down period the TPS23861 continues automatic operation starting with a detection cycle.

The TPS23861 will not automatically apply power to a port under the following circumstances:

- The detect status is not Resistance Valid.
- If the classification status is overcurrent, class mismatch, or unknown.

8.2.1 Kelvin Current Sensing Resistor

Load current in each PSE port is sensed as the voltage across a low-end current-sense resistor with a value of 255 mΩ. For more accurate current sensing, kelvin sensing of the low end of the current-sense resistor is provided through pins KSENSA for ports 1 and 2, and KSENSB for ports 3 and 4.

8.2.2 Connections on Unused Ports

The TPS23861 can be used on applications needing only 1 to 4 ports. On unused ports ground the SENx pin and leave the GATEx pin floating. DRAINx pins can be grounded or left open (leaving open may slightly reduce power consumption). One example of an unused PORT4 is shown in Figure 47. For detailed design and component selection information, see System Examples.

This schematic shows connections for an unused PORT4.

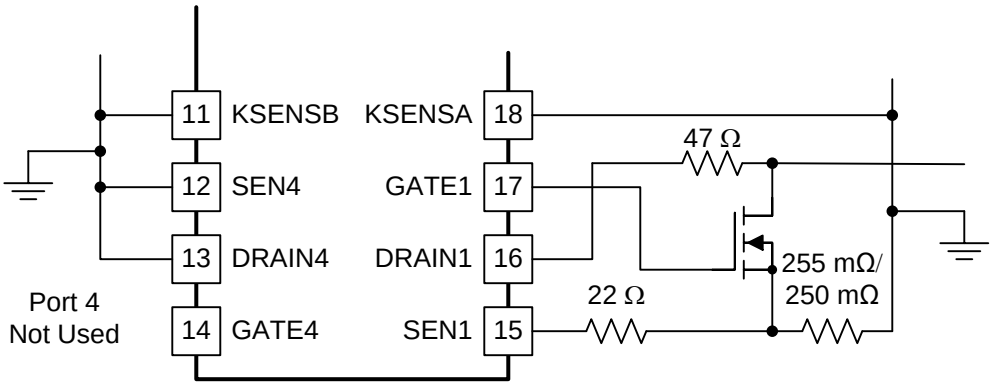


Figure 47. Unused PORT4 Connections

8.3 Typical Application

Typical applications are shown for several port counts. The TPS23861 is an effective choice for port counts less than the 4 ports provided, and these applications clearly show the connections for unused ports.

Applications are shown for both Auto Mode as well as Semi-Auto Mode. Operation in any mode except Auto Mode require I^2C host support. The TPS23861 provides useful telemetry in multi port applications to aid in implementing port power management.

8.3.1 Two Port, Auto Mode Application with External Port Reset

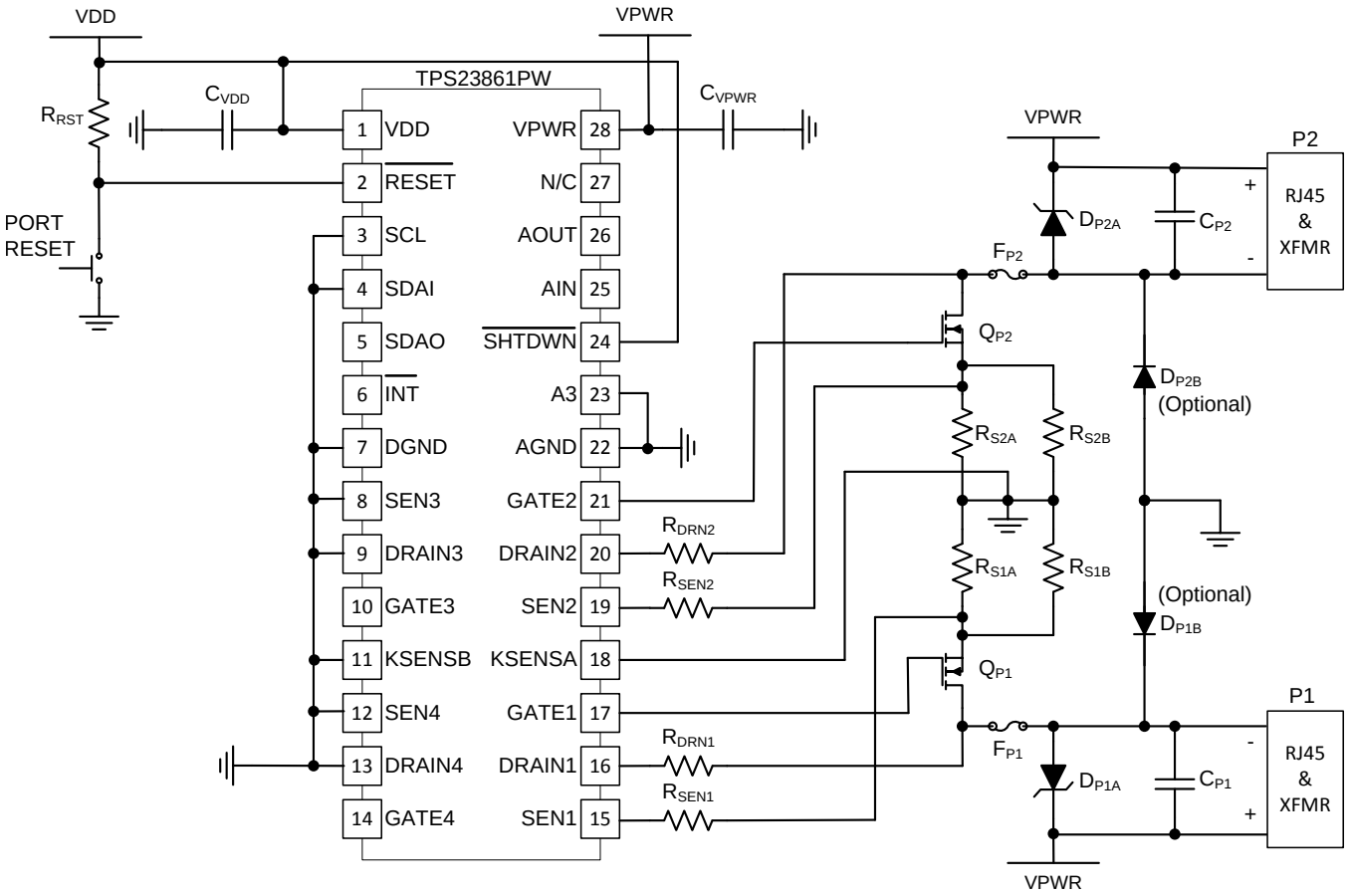


Figure 48. Two Port Auto Mode Application With Port Reset

8.3.1.1 Design Requirements

Table 12. Design Parameters

DESIGN PARAMETER	VALUE
Operating mode	Auto Mode
Number/type of ports	Two type 2 ports
Other requirements	Push button port reset

8.3.2 Four Port, Auto Mode Application

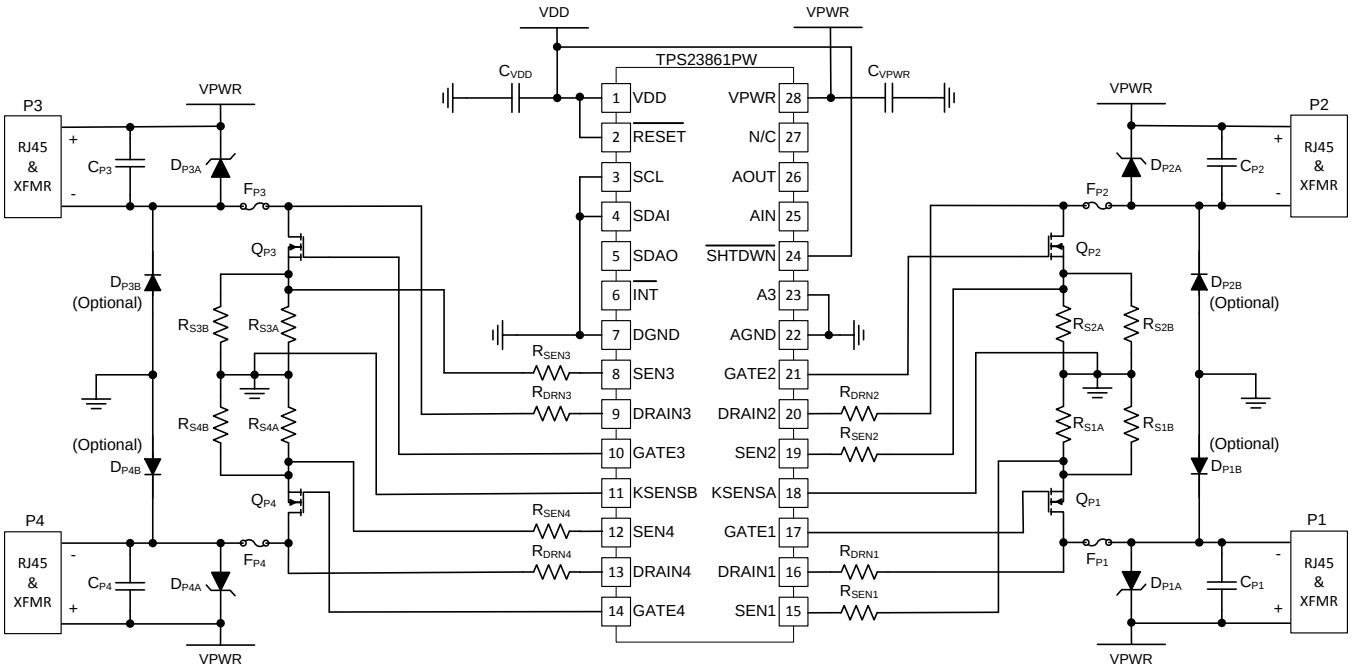


Figure 49. Four Port Auto Mode Application

8.3.2.1 Design Requirements

The design for the four port Auto Mode application is the same as for the two port design scaled up by two. In addition, the four port application does not require port reset so the $\overline{\text{RESET}}$ pin may be connected directly to VDD.

Table 13. Design Parameters

DESIGN PARAMETER	VALUE
Operating mode	Auto Mode
Number/type of ports	Four type 2 ports

8.3.3 Eight Port, Semi-Auto Mode Application Using MSP430 Micro-Controller

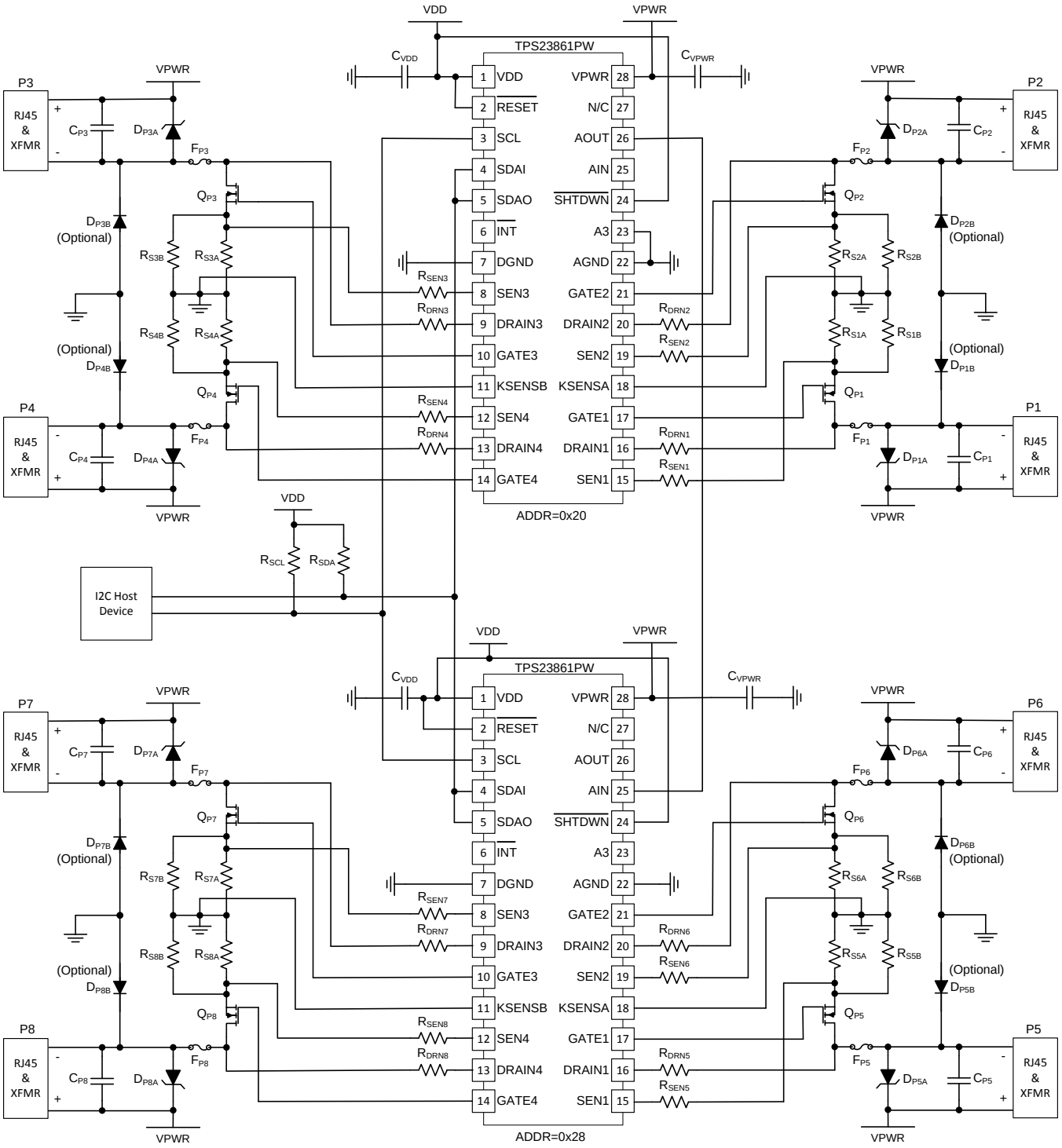


Figure 50. Eight Port Semi-Auto Mode Application

8.3.3.1 Design Requirements

The design for the eight port Semi-Auto Mode application is the same as for the two port design scaled up by four. In addition, the eight port application does not require port reset so the RESET pin may be connected directly to VDD. Two TPS23861 devices are used in the eight port configuration and are managed by the I^2C host device. The factory default I^2C address for each TPS23861 is 0x20 when the A3 pin is low and 0x28 when the A3 pin is left open or tied to VDD.

Table 14. Design Parameters

DESIGN PARAMETER	VALUE
Operating mode	Semi-Auto Mode
Number/type of ports	Eight type 2 ports
Other requirements	Micro-controller managed

8.3.4 Detailed Design Procedure

8.3.4.1 Power Pin Bypass Capacitors

- **C_{VPWR}:** 0.1 µF, 100 V, X7R ceramic at pin 28 (VPWR)
- **C_{VDD}:** 0.1 µF, 50 V, X7R ceramic at pin 1 (VDD)

8.3.4.2 Per Port Components

- **R_{DRNn}:** R_{DRNn} should be a 47-Ω, 5%, 0.1-W resistor in an 0603 SMT package.
- **R_{SENn}:** R_{SENn} should be a 22.1-Ω, 1%, 0.1-W resistor in an 0603 SMT package.
- **C_{Pn}:** 0.1-µF, 100-V, X7R ceramic between VPWR and Pn-
- **R_{SnA} / R_{SnB}:** The port current sense resistors can be either a combination of two 0.51-Ω, 1% resistors in parallel (0.255 Ω) or four 1.00-Ω, 1% resistors in parallel (0.250 Ω). The most common usage employs dual 0.51-Ω, 1%, 0.25-W resistors in an 0805 SMT package. Power dissipation for the resistor pair at maximum I_{CUT} is approximately 117 mW (~58 mW each).
- **Q_{Pn}:** The port MOSFET can be a small, inexpensive device with average performance characteristics.
  - BVDSS should be 100 V minimum for high voltage surge environment considerations.
  - $R_{DS(on)}$ (V_{GS} = 10 V) should be between 50 mΩ and 150 mΩ for power dissipation considerations.
    - The power dissipation for Q_{Pn} with $R_{DS(on)}$ = 100 mΩ at maximum I_{CUT} is approximately 46 mW.
  - Input capacitance (C_{ISS}) should be less than 2000 pF.
  - Gate Charge (Q_G) at V_{GATEn} = 12.5 V should be less than 50 nC (see NOTE below).

NOTE

For applications requiring faster response times under soft overload conditions (1 to 1.5 x ILIM), Q_G @ V_{GATEn} = 12.5 V may be required to be << 50 nC.

- **F_{Pn}:** The port fuse should be a slow blow type rated for at least 60 VDC and above ~2 x $I_{CUT(max)}$. The cold resistance should be below 200 mΩ to reduce the DC losses. The power dissipation for F_{Pn} with a cold resistance of 180 mΩ at maximum I_{CUT} is approximately 83 mW.
- **D_{PnA}:** The port TVS should be rated for the expected port surge environment. D_{PnA} should have a minimum reverse standoff voltage of 58 V and a maximum clamping voltage of 95 V at the expected peak surge current.
- **D_{PnB}:** The negative clamp diode is optional for extreme surge environments. D_{PnB} should be rated for V_R = 100 V minimum and be able to survive the expected surge current. Low forward voltage drop at the rated current is beneficial.

8.3.4.3 System Level Components (not shown in the schematic diagrams)

- **TVS:** The system TVS should have a minimum reverse standoff voltage of 58 V and a maximum clamping voltage of 95 V at the expected peak-surge current.
- **Bulk Capacitor:** The system bulk capacitor(s) should be rated for 100 V and can be an aluminum electrolytic type. Lower values can be paralleled to achieve at least 47 µF per four ports.
- **Digital I/O Pull-Up Resistors:** $\overline{\text{RESET}}$, AIN, A3, and $\overline{\text{SHTDWN}}$ are internally pulled up to VDD with a 50-kΩ (typical) resistor. A stronger pull-up resistor can be added externally such as a 10 kΩ, 1%, 0.063 W type in a SMT package. SCL, SDAI, SDAO, and $\overline{\text{INT}}$ require external pull-up resistors within a range of 1 kΩ to 10 kΩ depending on the total number of devices on the bus. The AOUT pin is either connected to an upstream device (to the AIN pin) or left unconnected and as such requires no external pull-up resistor.
- **Ethernet Data Transformer (per port):** The Ethernet data transformer must be rated to operate within the IEEE802.3at standard in the presence of the DC port current conditions. The transformer is also chosen to be compatible with the Ethernet PHY. The transformer may also be integrated into the RJ45 connector and cable terminations.
- **RJ45 Connector (per port):** The majority of the RJ45 connector requirements are mechanical in nature and include tab orientation, housing type (shielded or unshielded), or highly integrated. An integrated RJ45 consists of the Ethernet data transformer and cable terminations at a minimum. The integrated type may also contain the port TVS and common mode EMI filtering.
- **Cable Terminations (per port):** The cable terminations typically consist of series resistor (usually 75 Ω) and capacitor (usually 10 nF) circuits from each data transformer center tap to a common node which is then bypassed to a chassis ground (or system earth ground) with a high-voltage capacitor (usually 1000 pF to 4700 pF at 2 kV).

8.3.5 Application Curves

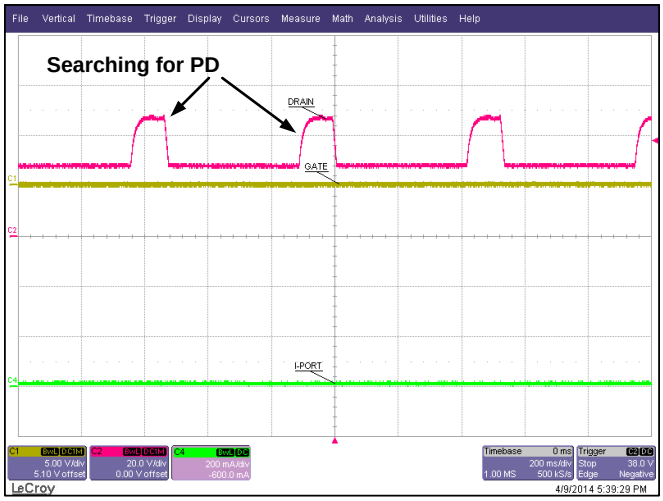


Figure 51.

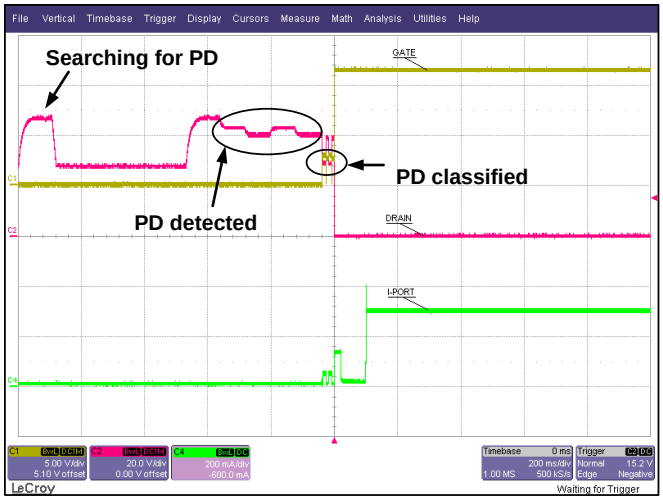


Figure 52.

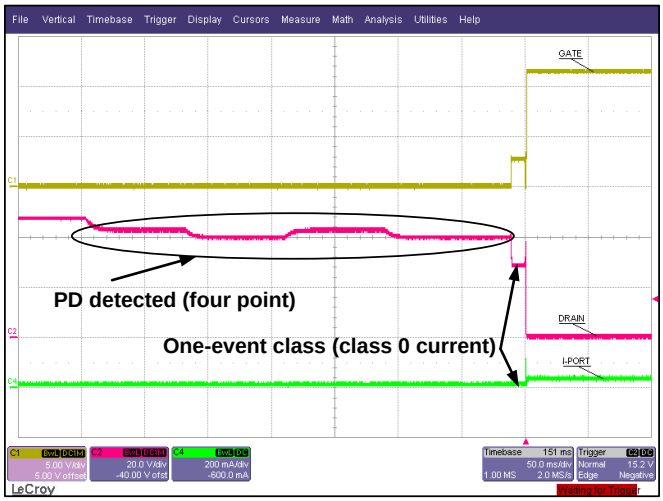


Figure 53.

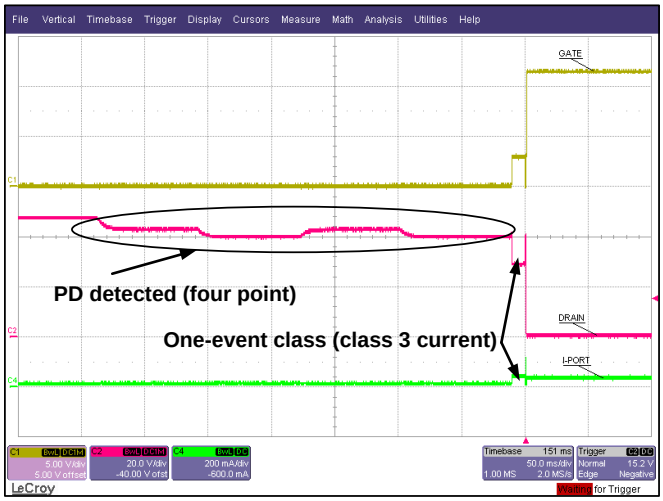


Figure 54.

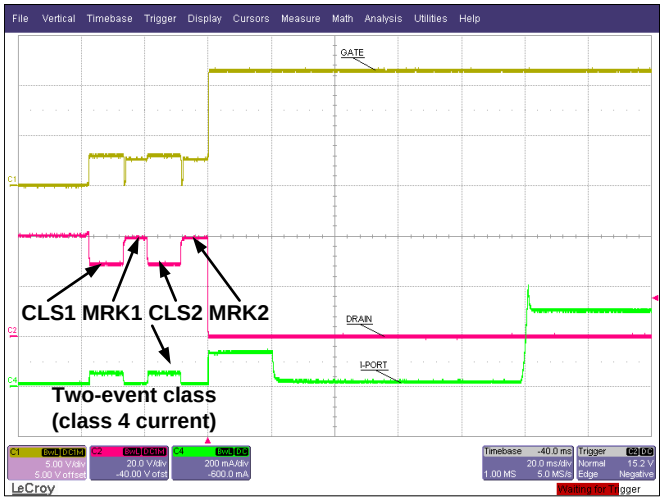


Figure 55.

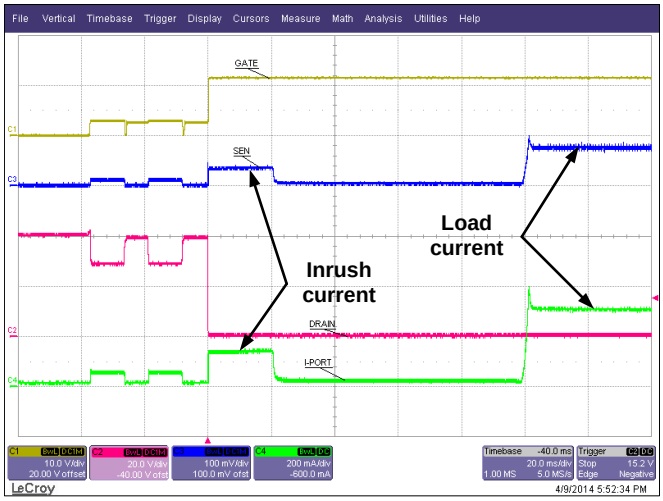


Figure 56.

8.4 System Examples

8.4.1 Overcurrent and Overload Protection

The TPS23861 provides three levels of overcurrent protection. During the t_{START} period immediately following power up, inrush current protection is provided as described in Inrush Protection. This protection allows the input capacitance of the PD to charge to the full input voltage on the power interface while ensuring the pass FET remains within its safe operating area.

Following the end of the t_{START} period a two-tiered current-limit protection scheme is applied to the ports. The first level (i.e., lower current) is the ICUT current limit. The ICUT current-limit threshold is set using the ICUTnm CONFIG registers and includes a timeout, t_{OVLD}, set using TICUT field in the TIMING CONFIGURATION register. When the TICUT timer times out because the ICUT current threshold is exceeded, the port is powered off, and the ICUTn bit in the FAULT EVENT register is set with the option of asserting an interrupt. This delay in powering down the port provides protection against spurious power downs during moderate load transients. See ICUT Current Limit.

The second level of powered-on current-limiting protection is the ILIM current limit. The ILIM current limit is a *hard limit*. That is, hardware protection including voltage foldback is imposed when the ILIM current threshold is reached. This second level of protection is invoked in the event of extreme overload or short circuit. The ILIM current-limit value is set using the POEPn bits in the PoE Plus register. Also, when the ILIM value is reached, the ILIM timer is started. When the ILIM timer times out, the port is powered off and the ILIMn bit in the Start/ILIM Event Register is set with the option of asserting an interrupt. See Foldback Protection (ILIM).

8.4.2 Inrush Protection

Inrush-current limiting is provided by the TPS23861 according to the curve in Figure 57. When the port is first powered on, the TSTART timer is started. While the TSTART timer is counting, the port current is limited to I_{INRUSH}, as shown in Figure 57. If at the end of t_{START} period the current is still limiting at I_{INRUSH}, the port is powered off and the STRTn bit in the Start/ILIM Event Register is set with the option of asserting an interrupt.

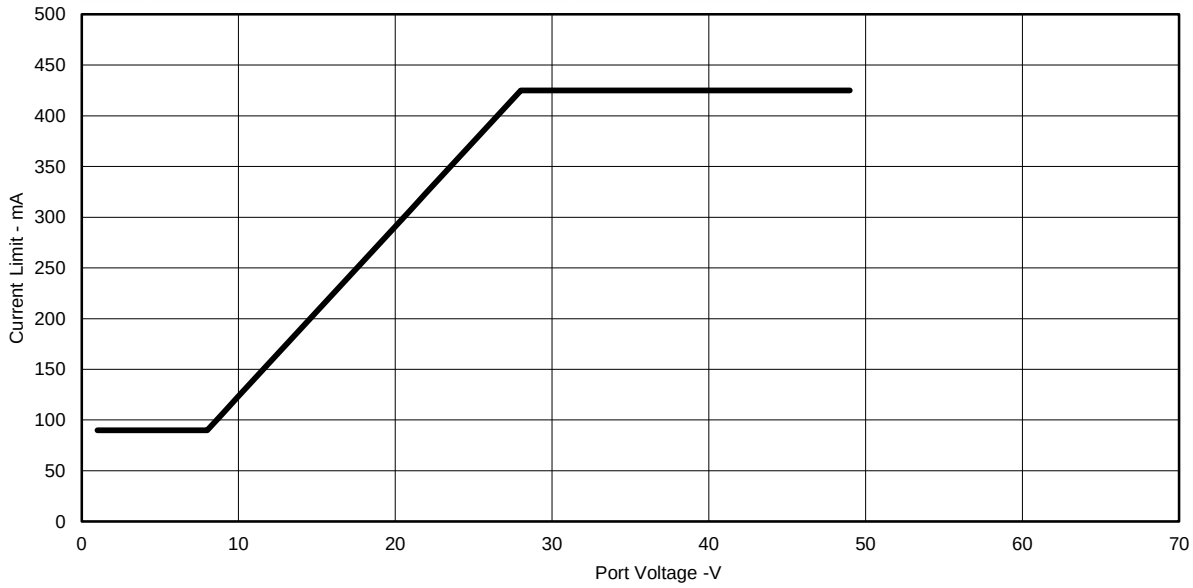


Figure 57. Foldback During Inrush (at port turn on)
I_{Inrush} vs V_{PORT}

System Examples (continued)

8.4.3 ICUT Current Limit

In addition to the absolute current limit imposed by the ILIM foldback curve (Figure 58) the TPS23861 supports an additional level of current-limit protection.

When the ICUT current-limit threshold is reached, the TICUT timer starts counting down. When it reaches zero the port is powered down. If the port current drops below the ICUT current-limit threshold while the TICUT timer is counting, the TICUT timer counts up, albeit at a slower rate, without exceeding the maximum count corresponding to the setting in the TICUT field.

The ICUT current-limit threshold is meant to be applied such that its setting is below the setting of the ILIM current limit. That is, the ICUT threshold should be reached before the TPS23861 asserts foldback control over the port current via an ILIM current limit. To this end, the ICUT threshold should be set lower than the ILIM current limit. This must be accomplished by the host except when in Auto Mode (or the AUTO bit is set). In that case, the settings for ICUT and ILIM is properly set based on classification results before the port is powered on.

The ICUT current limit threshold (ICUT) is programmable on a per-port basis in the 3-bit ICUT Port n fields in the ICUTnm CONFIG registers. The encoding of the ICUT Port n fields is shown in Table 15. The current values in Table 15 are nominal values.

Table 15. ICUT Current Limit Encoding

ICUT PORT n Field	ICUT (mA)	PoEPn (1)
000	374	0
001	110	0
010	204	0
011	374	0
100	754	1
101	592	1
110	645	1
111	920	1

(1) PoEPn bit should be set according to ICUT value for host to ensure the ICUT and ILIM relationship.

8.4.4 Foldback Protection (ILIM)

The TPS23861 features two types of foldback protection mechanisms for complete MOSFET protection. During inrush at port power on, the foldback is based on the port voltage as shown in Figure .

NOTE

The inrush-current profile remains the same no matter what the state is of the PoEPn bit in the PoE Plus Register.

After the port has been powered on and Power Good is valid, a dual-slope foldback current limit is applied, providing protection against partial and total short-circuit at port output, while still being able to maintain the port powered during normal transients in the TPS23861 input voltage or load current. Refer to Figure 58. Note that setting the POEPn bit selects the 2x curve while clearing it selects the 1x curve.

The TLIM timer starts counting down when the current-limit threshold in Figure 57 and Figure 58 is reached. When it reaches zero the port is powered down. If the ILIM current-limit condition is cleared while the TLIM timer is counting, the TLIM timer counts up, at a slower rate, without exceeding the maximum count corresponding to the setting in the TLIM field which is located in the Timing Configuration Register.

If the port experiences a short circuit, the TPS23861 forces zero volts on the gate of the external FET to protect it from destruction. Within microseconds the foldback circuit engages, and until the ILIM timeout is reached, the port current is controlled according to the foldback schedule.

The ILIM current limit is to be applied such that its setting is greater than the setting of the ICUT current threshold. That is, an ICUT current-limit condition should occur before the TPS23861 asserts foldback control over the port current via an ILIM current limit. To this end, the ILIM current limit must be set greater than the ICUT current threshold. This must be accomplished by the host except when in Auto Mode (or the AUTO bit is set). In that case, the settings for ICUT and ILIM will be properly set based on classification results before the port is powered on.

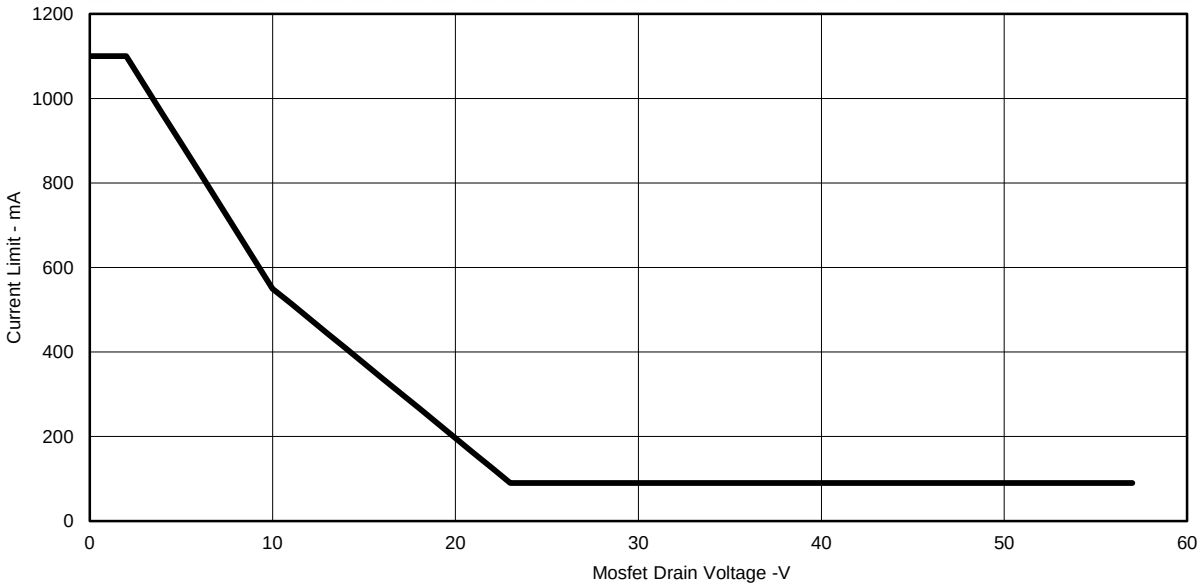


Figure 58. Foldback Port On (ILIM vs V_{DRAIN})

8.4.5 Kelvin Current Sensing Resistor

Load current in each PSE port is sensed as the voltage across a low-end current-sense resistor with a value of 255 mΩ. Alternatively, a 250-mΩ resistor may be used. If a 250-mΩ sense resistor is used the M250 bit in the General Mask 1 Register must be set. For more accurate current sensing, kelvin sensing of the low end of the current-sense resistor is provided through pins KSENSA for ports 1 and 2, and KSENSB for ports 3 and 4. Figure 59 illustrates the kelvin-sensing scheme.

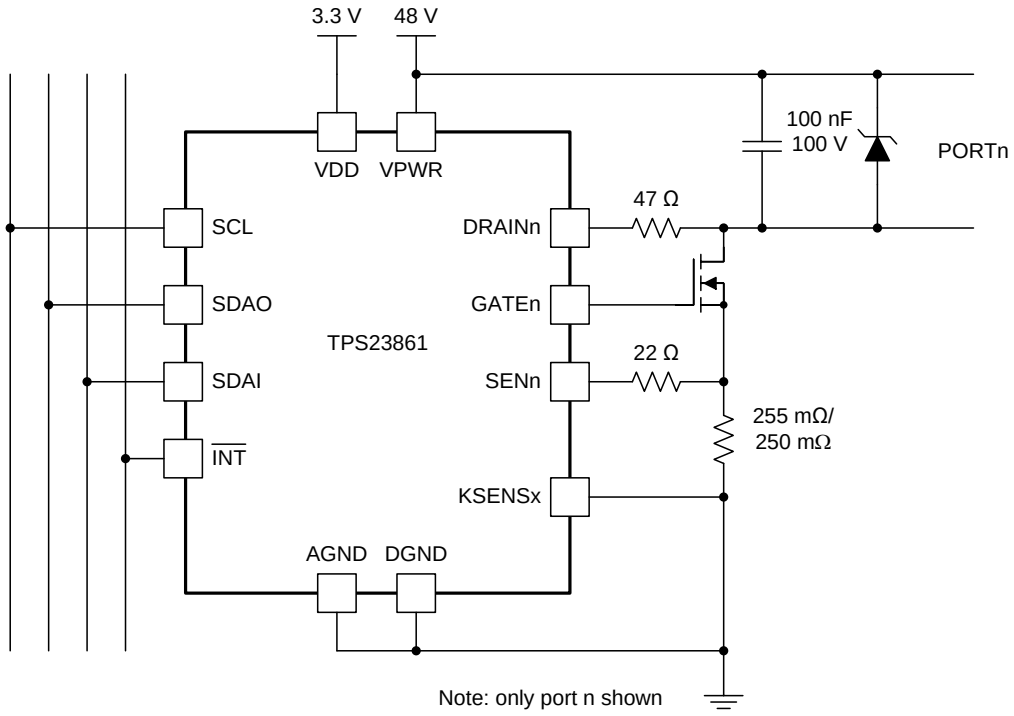


Figure 59. Kelvin Current-Sense Connection

9 Power Supply Recommendations

9.1 VDD

The recommended VDD supply voltage requirement is 3.3 V, ±0.3 V. Each TPS23861 requires approximately 5 mA typical and 6 mA maximum from the VDD supply. The VDD supply can be generated from VPWR with a linear regulator (TPS7A4001) for single TPS23861/Auto Mode based PSE or a buck-type regulator (LM5007 or LM5019 based) for a higher port count PSE using multiple TPS23861 devices operating in Auto or Semi-Auto Modes.

The power supply design must ensure the VDD rail rises monotonically through V_{UVDDR} without any droop below V_{UVDDF} as the loads are turned on. This is accomplished with proper bulk capacitance across the VDD rail for the expected load current steps over worst case design corners. Furthermore, the combination of decoupling capacitance and bulk storage capacitance must hold the VDD rail above the UVLO_fall threshold during any expected transient outages once power is applied.

9.2 VPWR

The recommended VPWR supply voltage requirement is 44 V to 57 V. A power supply with a nominal 48-V or 54-V output can support both type 1 and type 2 PD requirements. The output current required from the VPWR supply depends on the number and type of ports required in the system. The TPS23861 can be configured for type 1 and type 2 ports and the current limit is set proportionally. ICUT for a type 1 port is 374 mA , ±5%, and for a type 2 port is 645 mA, ± 5%. Size the VPWR supply accordingly for the number and type of ports to be supported. As an example, the VPWR power supply rating should be greater than 3.2 A for eight type 1 ports or greater than 5.5 A for eight type 2 ports, assuming maximum port and standby currents.

9.3 VPWR-RESET Sequencing

The voltage on the $\overline{\text{RESET}}$ pin (V_{RESET}) should be kept below 0.9 V until V_{VPWR} exceeds V_{UVLOPW_R}. If VDD is turned ON after V_{VPWR} exceeds V_{UVLOPW_R} then no delay for $\overline{\text{RESET}}$ is required. If VDD is ON before V_{VPWR} exceeds V_{UVLOPW_R} then a delay for $\overline{\text{RESET}}$ is required. This delay can be provided by the system host or with a capacitor (C_{RST}) connected to the $\overline{\text{RESET}}$ pin using the internal (50 kΩ typical) or external pullup resistor.

NOTE

For the schematic diagrams shown in Figure 36, Figure 46, Figure 48, Figure 49, and Figure 50, the VDD power supply is turned on after the VPWR power supply exceeds V_{UVLOPW_R}. More detail regarding TPS23861 power-on sequencing can be obtained by referring to the application note, TPS23861 Power-On Considerations, SLVA723.

10 Layout

10.1 Layout Guidelines

10.1.1 Port Current Kelvin Sensing

KSENSA is shared between SEN1 and SEN2, while KSENSB is shared between SEN3 and SEN4. In order to optimize the accuracy of the measurement, the PCB layout must be done carefully to minimize impact of PCB trace resistance. Refer to Figure 60 as an example.

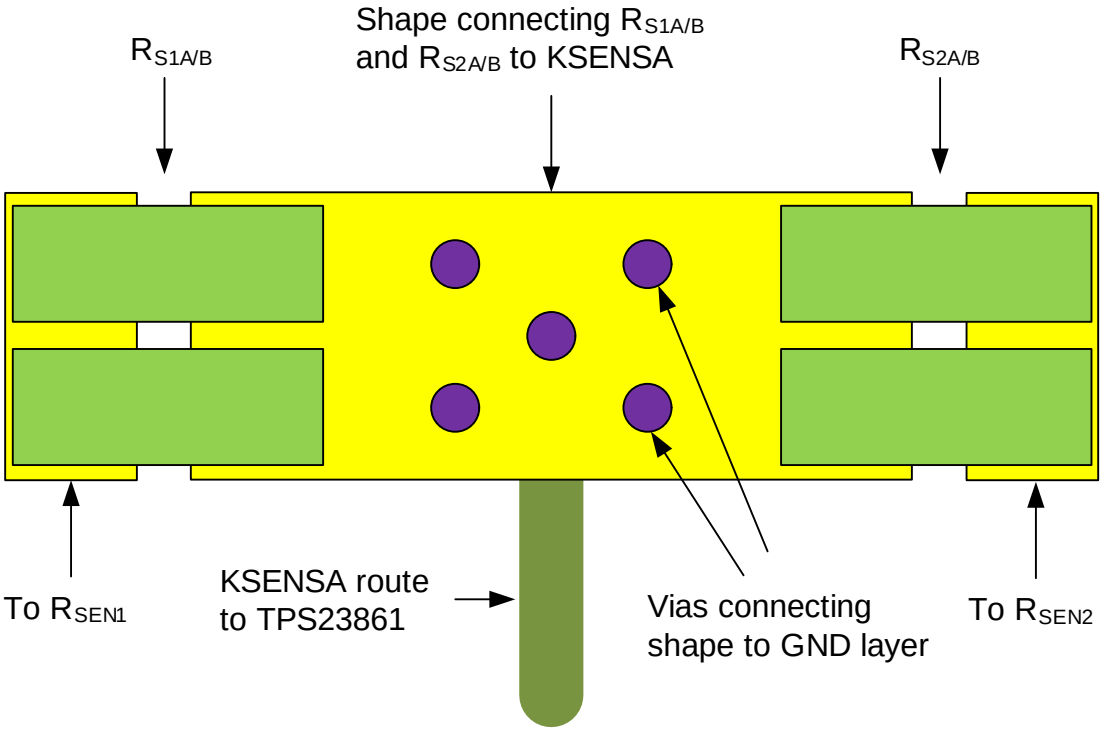


Figure 60. Kelvin Sense Layout Example

10.2 Layout Example

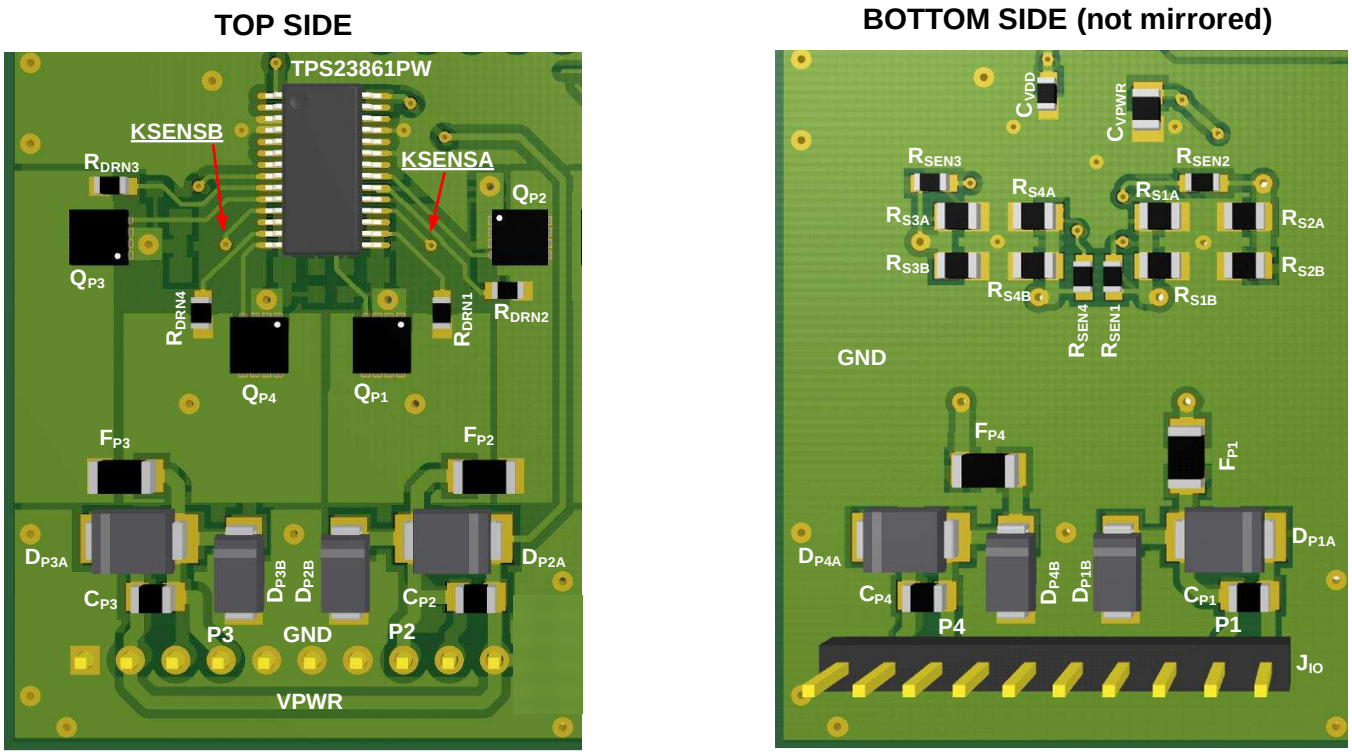


Figure 61. Four Port Layout Example

10.2.1 Component Placement and Routing Guidelines

10.2.1.1 Power Pin Bypass Capacitors

C_{VPWR}: Place close to pin 28 (VPWR) and connect with low inductance traces and vias according to Figure 61.

C_{VDD}: Place close to pin 1 (VDD) and connect with low inductance traces and vias according to Figure 61.

10.2.1.2 Per-Port Components

R_{SnA} / R_{SnB}: Place according to Figure 60 in a manner that facilitates a clean Kelvin connection with KSENSEA/B.

Q_{Pn}: Place Q_{Pn} around the TPS23861 as illustrated in Figure 61. Provide sufficient copper from Q_{Pn-D} to F_{Pn}.

R_{DRNn}: Place R_{DRNn} near to Q_{Pn-D}. Connect to DRAINn pins as illustrated in Figure 61.

R_{SENn}: Place R_{SENn} near to Q_{Pn-S}. Connect to SENn pins as illustrated in Figure 61.

F_{Pn}, C_{Pn}, D_{PnA}, D_{PnB}: Place this circuit group near the RJ45 port connector (or port power interface if a daughter board type of interface is used as illustrated in Figure 61). Connect this circuit group to Q_{Pn-D} / GND (TPS23861-AGND) using low inductance traces.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

IC Package Thermal Metrics application report, SPRA953.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS23861PW	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS23861PW	Samples
TPS23861PWR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS23861PW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

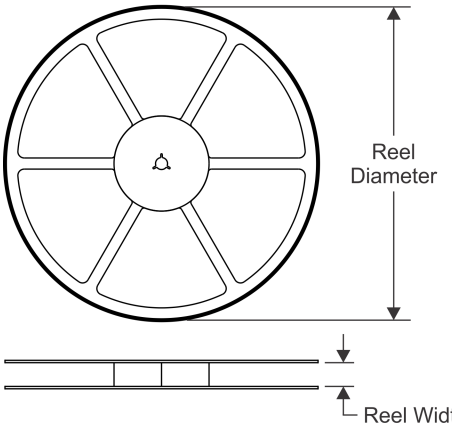
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

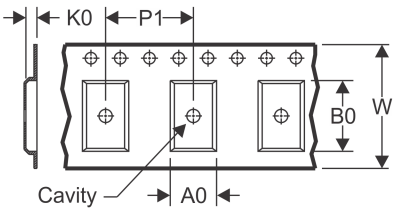
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

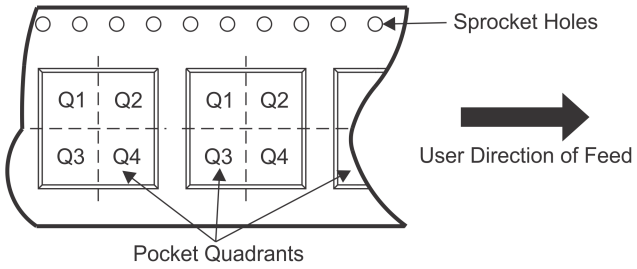


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

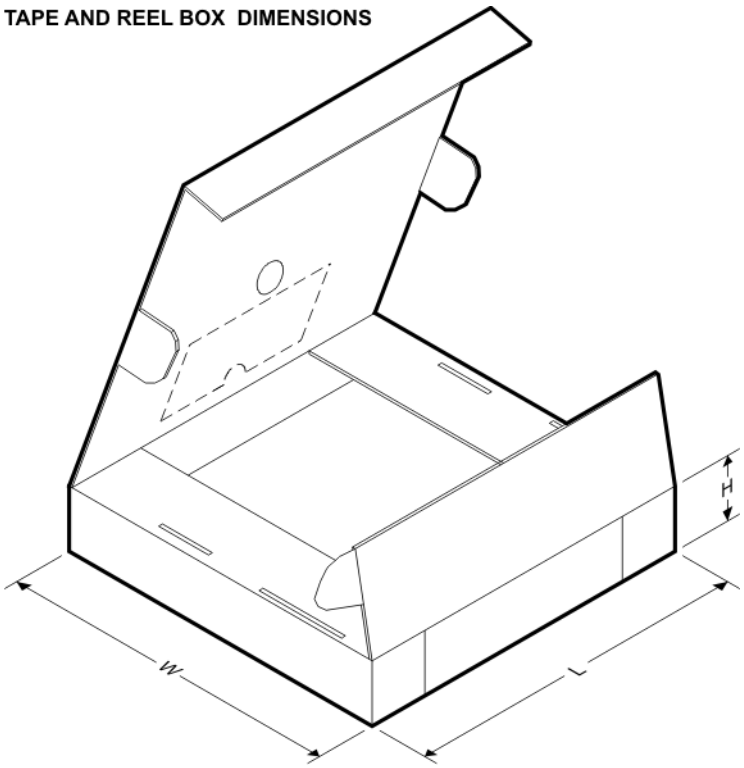
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS23861PWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

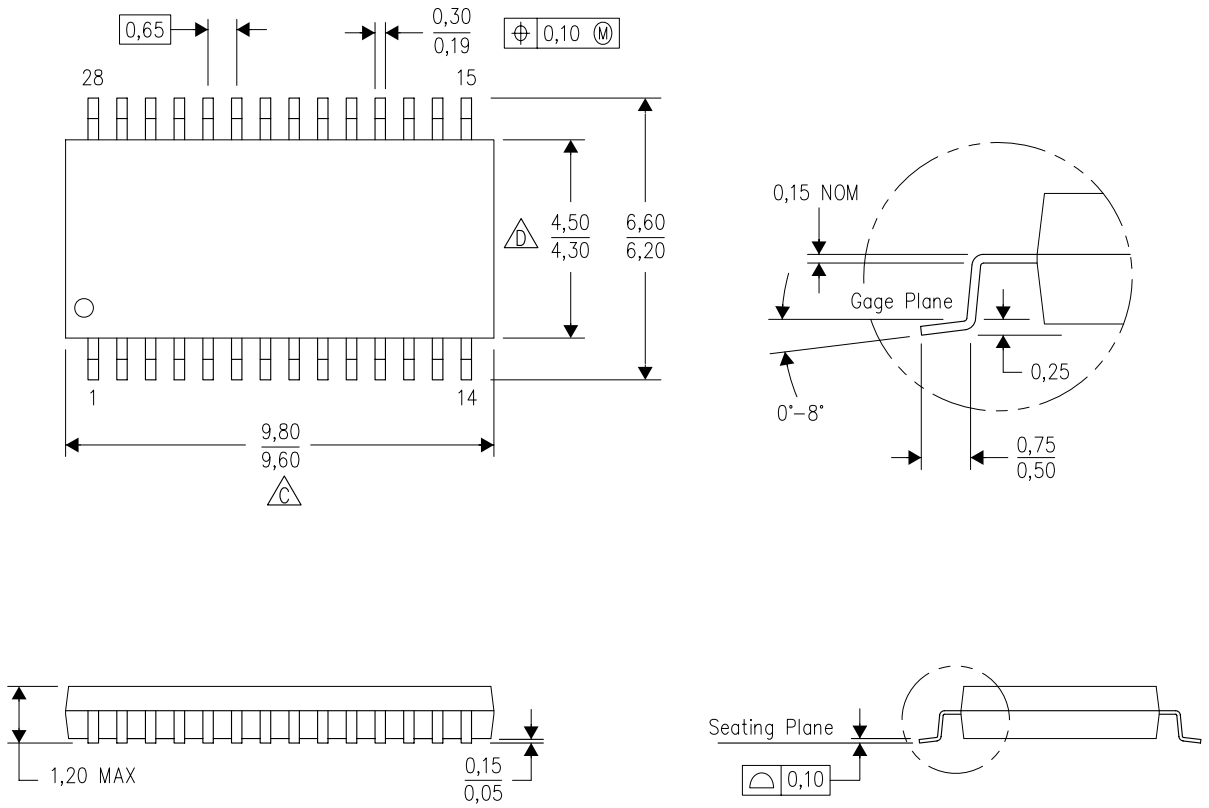
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS23861PWR	TSSOP	PW	28	2000	367.0	367.0	38.0

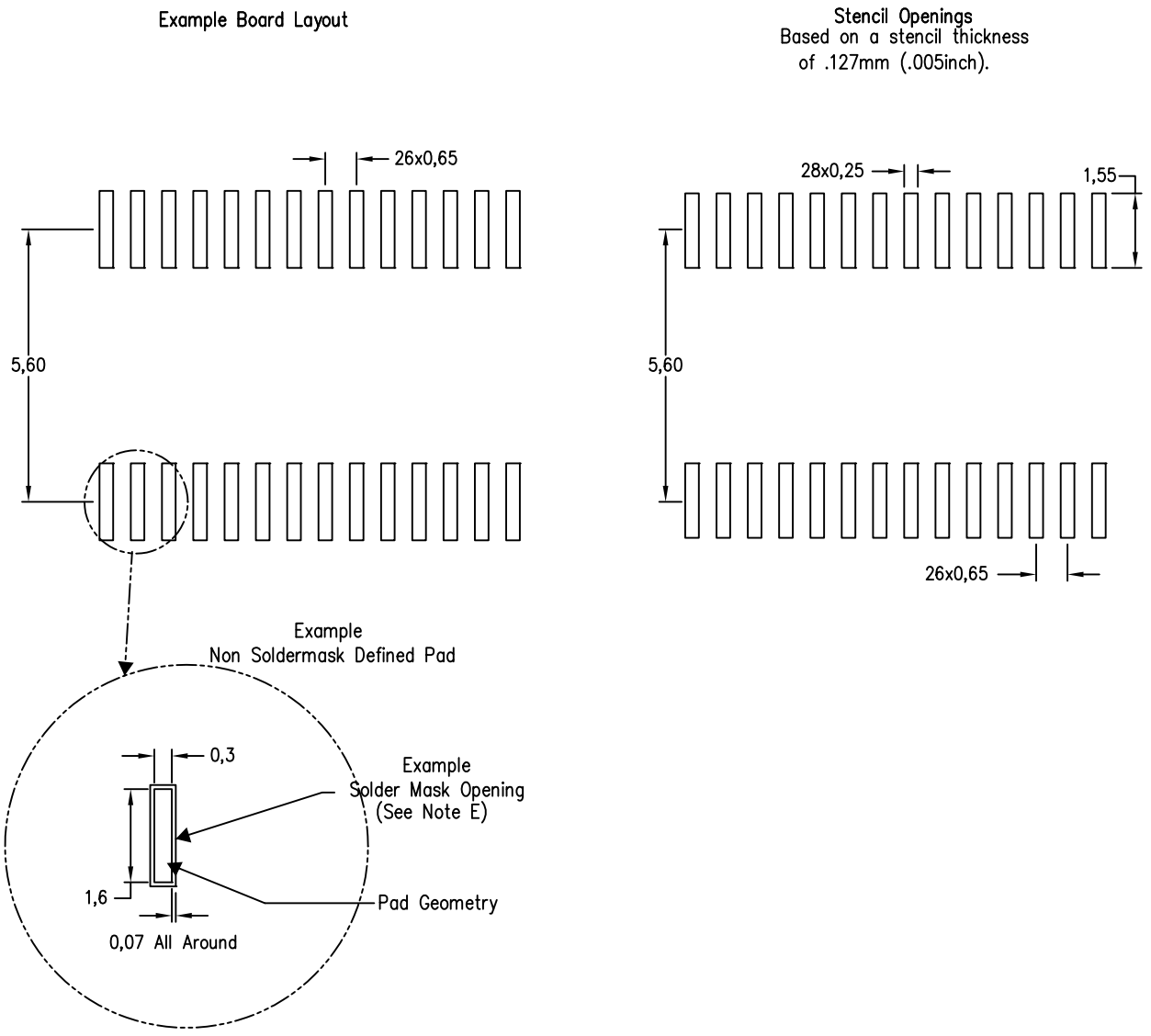
PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



4040064–7/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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